ACE Engineering Academy

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ESE- 2020 (Prelims) - Offline Test Series Test- 13

ELECTRONICS & TELECOMMUNICATION ENGINEERING

SUBJECT: CONTROL SYSTEMS, ANALOG ELECTRONICS & DIGITAL ELECTRONICS AND MICRO-PROCESSORS

01. Ans: (d)

Sol:
$$\frac{C}{R} = \frac{G_1G_2 + G_1G_3}{1-\left(-H_1G_1 - H_2G_2 + G_1G_3H_1H_2\right)}$$
$$\frac{C}{R} = \frac{G_1G_2 + G_1G_3}{1+H_1G_1 + H_2G_2 - G_1G_3H_1H_2}$$

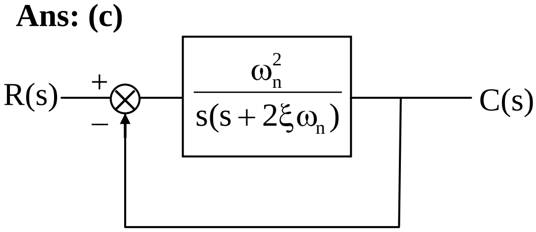
02. Ans: (a)

Sol: The main objective of drawing the root locus plots are

- To find out closed loop stability of system
- To find the range of K to make the system stable
- To find out relative stability of system
- To obtain a clear picture of the closed loop poles of the system
- To obtain a clear picture of the transient response of the system for varying gain K.
- To find out K-value for undamped, under damped, critical damped, over damped systems.

03. Ans: (c)

Sol:



CE = $s^2 + 4s + 4 = 0$

$\omega_n^2 = 4$

$\omega_n = 2$ rad/sec

04. Ans: (b)

Sol: PD controller is very sensitive to noise.

05. Ans: (b)

Sol: Since the value of resistance is independent of the frequency, the system is stable for all frequencies.

06. Ans: (a)

Sol: Angle condition

$$\angle G(s)H(s)\Big|_{s_1=-\frac{1}{2}+j\frac{\sqrt{3}}{2}} = \frac{\angle K}{\angle\left(-\frac{1}{2}+\frac{j\sqrt{3}}{2}+1\right)^3}$$
$$= \frac{\angle K}{\angle\left(\frac{1}{2}+\frac{j\left(\sqrt{3}\right)}{2}\right)^3}$$
$$= -3\tan^{-1}(\sqrt{3}) = -180^\circ$$

→ satisfies angle condition

→ s_1 is on root locus

$$\angle G(s)H(s)\Big|_{S_2=\left(-\frac{1}{2}+j\frac{1}{2}\right)} = \frac{\angle K}{\angle\left(-\frac{1}{2}+j\frac{1}{2}+1\right)^3}$$
$$= \frac{\angle K}{\angle\left(\frac{1}{2}+j\frac{1}{2}\right)^3}$$
$$= -3\tan^{-1}(1) = -135^\circ$$

→ Not satisfies angle condition

→ s_2 is not on Root Locus

07. Ans: (a)

Sol: $\xrightarrow{CE} 1+G(s)H(s)=0$

$\xrightarrow{CE} s^3 + 6s^2 + Ks^2 + 11s + 6 + K = 0$

$\xrightarrow{CE} (s^3 + 6s^2 + 11s + 6) + K(s^2 + 1) = 0$

$$G(s)\,H(s) = \frac{K(s^2+1)}{s^3+6s^2+11s+6}$$

No. of Asymptotes N = |P – Z| = |3 – 2| = 1

$$\theta_0 = \frac{(2\ell+1)180^\circ}{(P-Z)} = \frac{(2\times 0+1)180^\circ}{1} = 180^\circ$$

08. Ans: (d)

Sol: Option (a) is lag compensator which is wrong

Options (b), (c) & (d) are lead compensators.

Here required to verify stability with Gain K

$$G(s) = \frac{1}{s-1},\ G_c(s) = K\left(\frac{s+2}{s+10}\right)$$

$$G(s)\Big|_{\omega_c} = \frac{K(s+2)}{(s-1)(s+10)},\ H(s) = 1$$

$\xrightarrow{CE} 1 + G(s)\Big|_{\omega_c} = 0$

$\xrightarrow{CE} s^2 + 10s - s - 10 + Ks + 2K = 0$

$\xrightarrow{CE} s^2 + 9s - 10 + Ks + 2K = 0$

$\xrightarrow{CE} s^2 + s(K + 9) + (2K - 10) = 0$

s^2	1	2K – 10
s^1	(K + 9)	
s^0	(2K – 10)	

$(K+9) > 0 \Rightarrow K > -9$,

$(2K-10) > 0 \Rightarrow K > 5$

K > 5 Given system with lead compensator becomes stable. Option (d) is correct

09. Ans: (a)

Sol: $$\alpha = \frac{R_2}{R_1+R_2} = \frac{1}{1+1} = \frac{1}{2}$$

$$\phi_m = \sin^{-1}\left(\frac{1-\alpha}{1+\alpha}\right) = \sin^{-1}\left(\frac{1-\frac{1}{2}}{1+\frac{1}{2}}\right)$$

$$= \sin^{-1}\left(\frac{1}{3}\right)$$

10. Ans: (c)

Sol: If the poles are located in left side of s - plane, then the system is stable. (or)

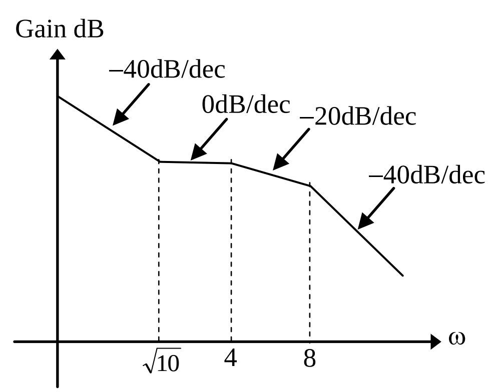
The IR of a causal and stable system must be absolutely integrable between the limits 0 and ∞ $\int_0^\infty |IR|\,dt < \infty$

If the roots are located on imaginary axis which are repeated then the system is unstable. $\int_0^\infty |IR|\,dt = \infty$

When non-repeated or simple poles poles are located on imaginary axis, then the system is marginally or limitedly or critically or just stable (or) When time $t \to \infty$ IR is neither approaches to '0' nor goes to '∞' and will have fixed IR.

11. Ans: (d)

Sol:



$\omega = 0 \quad \angle TF = -180^\circ$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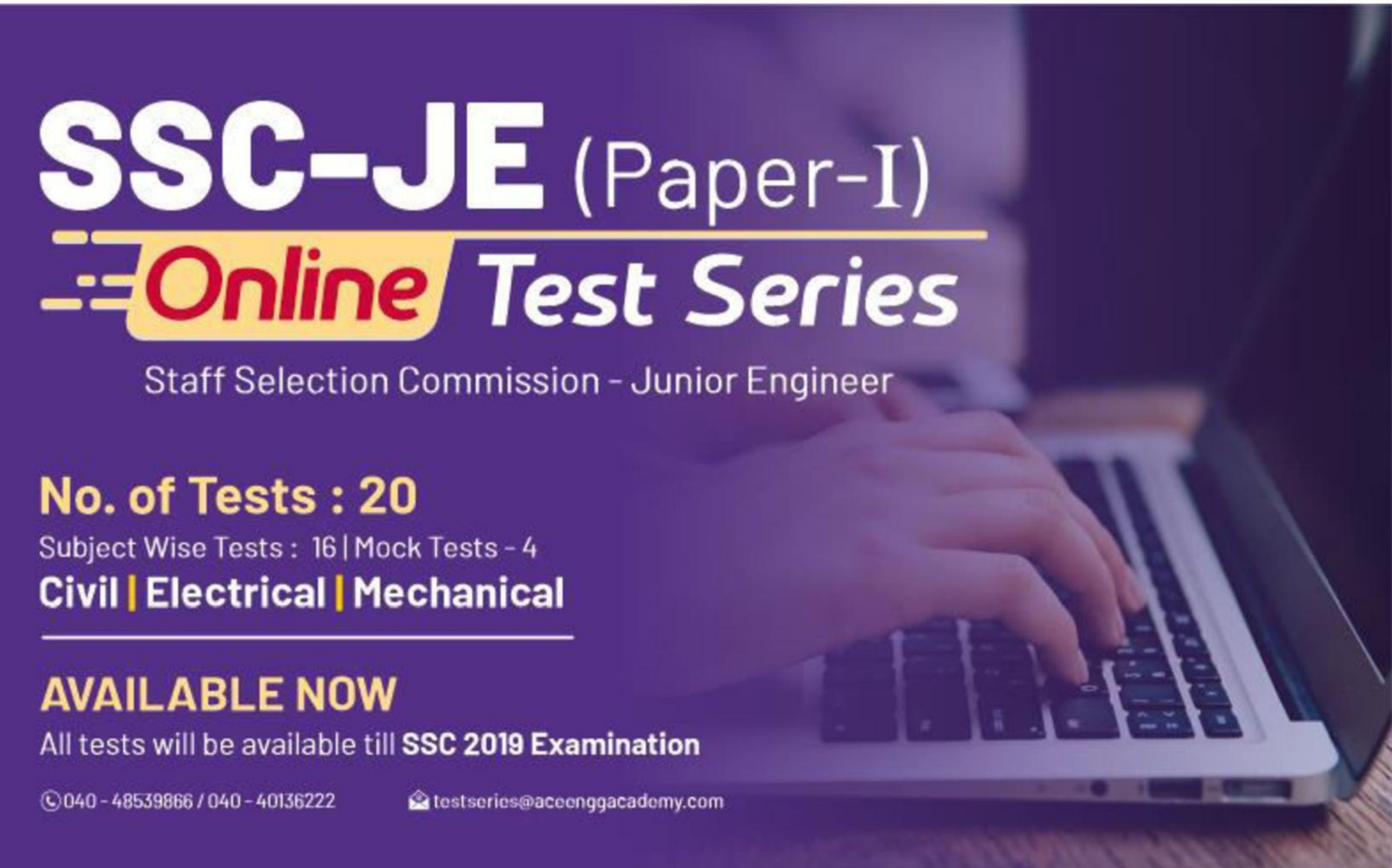
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12. Ans: (c)

Sol: $\angle \dfrac{e^{\frac{-\pi}{2}j\omega}}{j\omega} = -\pi$

$-\left(\dfrac{\pi}{2}\omega + \dfrac{\pi}{2}\right) = -\pi$

$\omega_{pc} = 1$ rad/sec

$\left|\dfrac{e^{\frac{-\pi}{2}j\omega}}{j\omega}\right| = \dfrac{1}{\omega} = 1$

$\therefore$ GM = 1 or 0 dB

$\left|\dfrac{e^{\frac{-\pi}{2}j\omega}}{j\omega}\right| = 1$

$\omega_{gc} = 1$ rad/sec

$\text{PM} = 180° - 90° - \dfrac{\pi}{2}\omega_{gc}$

$= 180° - 90° - 90° = 0°$

PM = 0°

13. Ans: (a)

Sol: $G(s) = \dfrac{8}{(S+10)^2}$

$S = j\omega$

$G(j\omega) = \dfrac{8}{(j\omega+10)^2}$

$|G(j\omega)| = \dfrac{8}{\left(\sqrt{\omega^2+10^2}\right)^2}$

O/p amplitude = I/p amplitude × $|G(\omega)|$

$= 2.\dfrac{8}{\left(\sqrt{\omega^2+10^2}\right)^2}$

Where $\omega = 3$ rad/sec

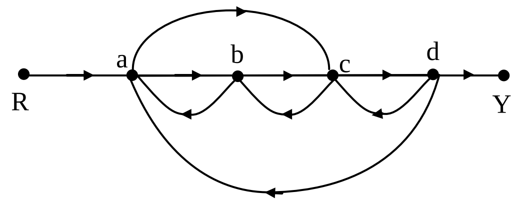
$\text{o/p amplitude} = \dfrac{2\times 8}{\left(\sqrt{100+9}\right)^2}$

$= \dfrac{16}{109}$

$= 0.146$

14. Ans: (a)

Sol:



Number of forward paths = 2

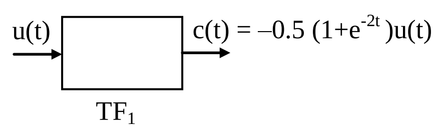
RabcdY, RacdY

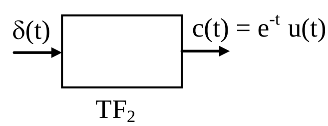
Number of two non touching loops = 1

aba, cdc

15. Ans: (a)

Sol:





$TF_1 = \dfrac{L.T\left[-0.5\left(1+e^{-2t}\right)\right]}{L.T[u(t)]}$

$= \dfrac{-0.5\left(\dfrac{1}{s}+\dfrac{1}{s+2}\right)}{\dfrac{1}{s}} = \dfrac{-(s+1)}{s+2}$

$TF_2 = \dfrac{1}{s+1}$

Overall transfer function of system

$TF = TF_1.TF_2 = \dfrac{-1}{s+2}$

16. Ans: (c)

Sol: There are two loops

Loop gain 1 = – $H_1G_1G_2$

Loop gain 2 = – $H_2\,G_3$

17. Ans: (d)

Sol: $TF = \dfrac{R+\dfrac{1}{Cs}}{R+Ls+R+\dfrac{1}{Cs}} = \dfrac{RCs+1}{LCs^2+2RCs+1}$

2 poles, 1 zero.

18. Ans: (b)

Sol: CE $\rightarrow s^2 + 3s + 2 = 0$

From above equation,

$2\xi\omega_n = 3$ and $\omega_n = \sqrt{2}$

$\Rightarrow \xi = \dfrac{3}{2\sqrt{2}} > 1 \Rightarrow$ over damped

$C(0) = \underset{s\to\infty}{\text{Lt}}\, sC(s) = \underset{s\to\infty}{\text{Lt}} \dfrac{2}{(s+1)(s+2)} = 0$

Final value

$C(\infty) = \underset{s\to 0}{\text{Lt}} \dfrac{2}{(s+1)(s+2)} = 1$

19. Ans: (c)

Sol: The bandwidth for first order system,

$BW = \dfrac{1}{T}$, Here 'T' is time constant

OLTF: $G(s) = \dfrac{1}{s+1}$

$G(s) = \dfrac{1}{sT+1}$

Time constant, T = 1

Bandwidth = G(s) = $\dfrac{1}{1}$ = 1 rad/s

$CLTF = \dfrac{1}{s+2} = \dfrac{\frac{1}{2}}{1+\frac{s}{2}}$

$T = \dfrac{1}{2}$

Bandwidth = $\dfrac{1}{T}$ = 2 rad/s

20. Ans: (a)

Sol:

$+x^6$	1	–2	–16	32
$+x^5$	1	0	–16	0
$-x^4$	–2	0	32	
$-x^3$	0(–8)	0	0	
$+x^2$	0(ε)	32		
$+x^1$	$\dfrac{(32)(8)}{\varepsilon}$			
$+x^0$	32			

$AE = -2x^4 + 32$

$\dfrac{\partial AE}{\partial x} = -8x^3$

No. of RH roots = 2

jω roots = 2

LH roots = 2

21. Ans: (a)

Sol: Delay time → 0 to 50% of the final value

Rise time → 10 to 90% of the final value

22. Ans: (b)

Sol: $T(s) = \dfrac{C(s)}{R(s)} = \dfrac{G(s)}{1+G(s)H(s)}$

$= \dfrac{\dfrac{K(s+4)}{s(s+1)}}{1+\dfrac{1}{s+2}.\dfrac{K(s+4)}{s(s+1)}}$

$= \dfrac{K(s+4)(s+2)}{s(s+1)(s+2)+K(s+4)}$

C.E = 1+ G(s)H(s) = 0

$s^3 + 3s^2 + 2s + Ks + 4K = 0$

$s^3 + 3s^2 + (2+K)s + 4K = 0$

RH table:

s^3	1	2+K
s^2	3	4K
s^1	$\frac{6+3K-4K}{3}$	
s^0	4K	

For marginal stable: s^1-row must be zero

$$\frac{6-K}{3}=0$$

K = 6

23. Ans: (a)

Sol: $$T.F=\frac{L[\text{output}]}{L[\text{input}]}=\frac{L[c(t)]}{L[\text{unit step}]}$$

$$=\frac{L\left[1-e^{-10t}-10t\,e^{-10t}\right]}{L[u(t)]}$$

$$=\frac{\frac{1}{s}-\frac{1}{s+10}-\frac{10}{(s+10)^2}}{\frac{1}{s}}$$

$$\Rightarrow\frac{C(s)}{R(s)}=\frac{100}{s^2+20s+100}=\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$$

ω_n = 10 rad/sec; $2\zeta\omega_n = 20$

$2\zeta(10) = 20$

$\zeta = 1$

Impulse response in time domain

$= L^{-1}$ [transfer function]

$$= L^{-1}\left[\frac{100}{s^2+20s+100}\right]$$

$$=L^{-1}\left[\frac{100}{(s+10)^2}\right]=100\ t\ e^{-10t}$$

24. Ans: (b)

Sol: Given $A_v = 100$, $Z_i = 1k\Omega$, $Z_0 = 5k\Omega = Z_L$

Current-Shunt Negative feedback Amplifier gain is Current gain.

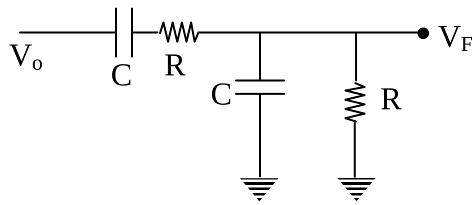
$$A_v=\frac{A_I.Z_L}{Z_i}\Rightarrow A_I=\frac{A_v.Z_i}{Z_L}=\frac{100\times1}{5}=20$$

$1 + \beta A_I = 1 + 0.2\ (20) = 5$

$$Z_{if}=\frac{Z_i}{1+\beta A_I}=\frac{1}{5}k\Omega$$

25. Ans: (b)

Sol: The feedback circuit of Wein Bridge oscillator is as below.



$$\frac{V_F-V_o}{R+\frac{1}{SC}}+SCV_F+\frac{V_F}{R}=0$$

$$V_F\left(\frac{1}{R+\frac{1}{SC}}+SC+\frac{1}{R}\right)=\frac{V_o}{R+\frac{1}{SC}}$$

$$\frac{V_o}{V_F}=1+SC\left(R+\frac{1}{SC}\right)+\frac{1}{R}\left(R+\frac{1}{SC}\right)$$

$$= 1+SCR + 1 + 1 + \frac{1}{SCR}$$

$$= 3 + SCR + \frac{1}{SCR}$$

$$\Rightarrow\frac{V_o}{V_F}=3+j\left(\omega RC-\frac{1}{\omega RC}\right)$$

At resonant frequency

$\frac{V_o}{V_F}=3$ ($\because$ Imaginary part is zero)

$\therefore$ Attention factor (or) feedback factor,

$$\beta=\frac{V_F}{V_o}=\frac{1}{3}$$

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26. Ans: (c)

Sol: Given A = 300, D = 16% , $\beta = \frac{5}{100}$

$$1+\beta A = 1+\frac{5}{100}\times 300 = 16$$

$$D_f = \frac{D}{1+\beta A} = 1\%$$

27. Ans: (b)

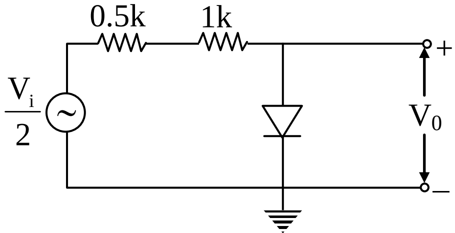
Sol:
1. Reverse bias is applied between gate and source ⇒ High input resistance in a FET amplifier
2. Minority carrier current is almost zero ⇒ Good bias stability
3. In FET's and MOSFET's voltage gain is very less because A_V is a function of g_m but $g_m \propto I_D$. Since the channel width is narrow, I_D is small ⇒ Gain bandwidth product is low
4. Total current is contributed by majority carriers and more over there were no junctions in the current flowing path from source to drain ⇒ lower noise

28. Ans: (c)

Sol: Feedback factor $\beta = \frac{-C_1}{C_2} = \frac{-180}{18} = -10$

29. Ans: (d)

Sol: The equivalent circuit is



When $\frac{V_i}{2} > 0.7V$

D-ON ⇒ V_0 = 0.7V

When $\frac{V_i}{2} \le 0.7V$

D-OFF ⇒ $V_0 = \frac{V_i}{2}$ = 2.5sinωt

⇒ $V_{0\,min}$ = –2.5V

∴ $(V_0)_{max}$ = 0.7V , $(V_0)_{min}$ = –2.5V

30. Ans: (b)

Sol: Input power = $V_i \times I_i$

= $0.5 \times 2 \times 10^{-3}$ = 1mW

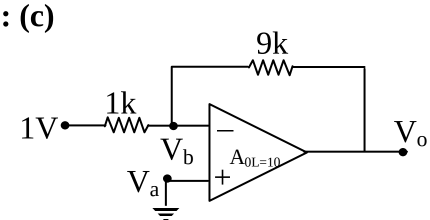
Output power = $V_0 \times I_0 = 16 \times 15 \times 10^{-3}$

= 240mW

Power gain = $\frac{P_0}{P_i} = 240$

31. Ans: (c)

Sol:



$$V_b = \frac{V_0(1k)+(1V)(9k)}{10k}$$

$$V_b = \frac{V_0+9}{10}$$

$$V_0 = A(V_a - V_b)$$

$$V_0 = 10\left(0-\frac{V_0+9}{10}\right)$$

$$V_0 = -V_0 - 9$$

$$2V_0 = -9$$

$$\therefore V_0 = -4.5\text{Volts}$$

32. Ans: (a)

Sol:

→ A BJT acts as amplifier in active region

→ Transformer coupling reduces the number of stages for achieving same power gain as compared to RC coupled stages.

→ Direct coupling is preferred to amplify DC and low frequency signals

33. Ans: (c)

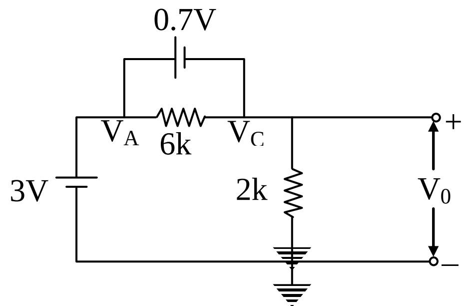
Sol: When diode is OFF,

$$V_0 = 3\left(\frac{2k}{2k+6k}\right) = 0.75V$$

$V_A = 3V$, $V_C = 0.75V$,

$\Rightarrow V_D = V_A - V_C = 2.25V$

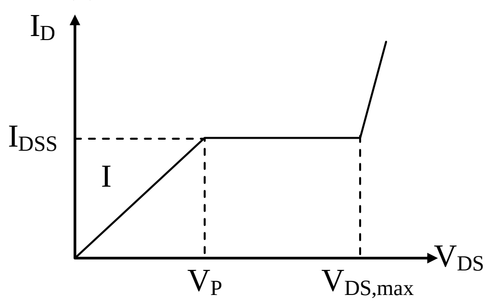
So, $V_A > V_C \Rightarrow$ Then Diode is ON.



$\therefore V_0 = 3 - 0.7 = 2.3V$

34. Ans: (c)

Sol:



JFET operating in region 'I' if $I_D < I_{DSS}$, I_D is linearly related to V_{DS}, so it behaviour like a resistor.

35. Ans: (c)

Sol: → Placing a BJT around an op-amp provides a logarithmic function.

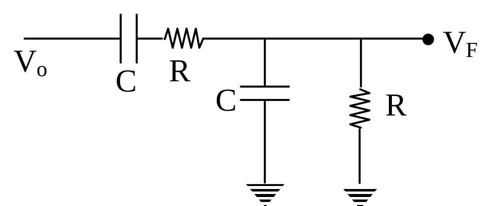
→ Placing a diode around an op-amp leads to precision rectifier i.e., a circuit that can rectify very small input swings.

→ Integrators suffer from op-amp imperfections like DC offsets and input bias currents.

→ The speed of op-amp circuits is limited by the bandwidth of the op-amps. For large signals, the op-amp suffers from a finite slew rate, distorting the output waveform.

36. Ans: (c)

Sol: The feedback circuit of Wein Bridge oscillator is as below



$$\frac{V_F - V_o}{R + \frac{1}{SC}} + SCV_F + \frac{V_F}{R} = 0$$

$$V_F\left(\frac{1}{R+\frac{1}{SC}} + SC + \frac{1}{R}\right) = \frac{V_o}{R+\frac{1}{SC}}$$

$$\frac{V_o}{V_F} = 1 + SC\left(R + \frac{1}{SC}\right) + \frac{1}{R}\left(R + \frac{1}{SC}\right)$$

$$= 1 + SCR + 1 + 1 + \frac{1}{SCR} = 3 + SCR + \frac{1}{SCR}$$

$$\Rightarrow \frac{V_o}{V_F} = 3 + j\left(\omega RC - \frac{1}{\omega RC}\right)$$

Feedback factor

$$\beta = \frac{V_F}{V_o} = \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega CR}\right)}$$

At frequency of Oscillations, imaginary part is zero, $\beta = 1/3$, $A = 3$

37. Ans: (c)

Sol: Frequency of oscillations generated by the Wein bridge oscillator is

$$f = \frac{1}{2\pi\sqrt{(R_1C_1)(R_2C_2)}}$$

given $R_1 = 4R$, $R_2 = R$, $C_1 = C$, $C_2 = 4C$

$$f = \frac{1}{2\pi\sqrt{(4RC)(4RC)}} = \frac{1}{8\pi RC}$$

38. Ans: (b)

Sol: The given circuit is a voltage regulator. Then

(i) The unregulated input voltage, V_S should be more than the break down voltage of zener diode, V_Z

(ii) By applying KCL at node A in the circuit, $I_1 = I_2 + I_L \Rightarrow I_L = I_1 - I_2$

(iii) The dynamic resistance of zener diode r_z when it is in break down is very small when compared with the resistance R_S.

i.e R_S should be more than r_z, so that it maintains the current into zener diode between $I_{Z_{min}}$ and $I_{Z_{max}}$

39. Ans: (b)

Sol: A. E-B junction forward bias and C-B junction reverse bias-High gain amplifier

B. Both E-B and C-B junctions forward bias- Saturation condition

C. E-B junction reverse bias and C-B junction forward bias- Very low gain amplifier

D. Both E-B and C-B junctions reverse bias- Cut-off condition

40. Ans: (b)

Sol: $I_{CQ} = \dfrac{V_{CC}}{R_{AC} + R_{DC}} = \dfrac{V_{CC}}{R_C + R_C} = \dfrac{V_{CC}}{2R_C}$

41. Ans: (a)

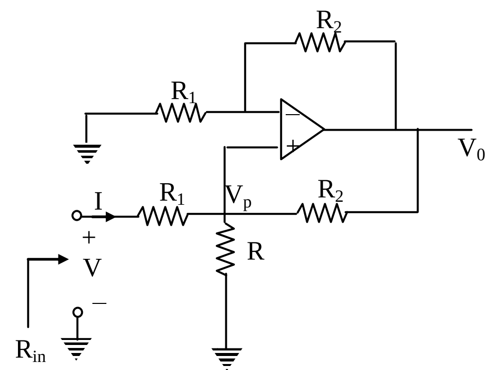
Sol: Astable Multivibrator can generate square waveforms.

Mono stable Multivibrator is used for pulse width modulation.

Bi-stable Multivibrator is using to storing binary information.

42. Ans: (d)

Sol:



$$\frac{V_oR_1}{R_2 + R_1} = V_P \rightarrow V_O = V_P\left[1 + \frac{R_2}{R_1}\right]$$

$$\rightarrow V_P - V_o = -\frac{V_PR_2}{R_1}$$

KCL at non inverting terminal

$$\frac{V_P - V}{R_1} + \frac{V_P}{R} + \frac{V_P - V_0}{R_2} = 0$$

$$\frac{V_P - V}{R_1} + \frac{V_P}{R} - \frac{V_P}{R_1} = 0$$

$$V_P\left[\frac{1}{R_1} - \frac{1}{R_1} + \frac{1}{R}\right] = \frac{V}{R_1}$$

$$V = V_P\left[\frac{R_1}{R}\right]$$

$$I = \frac{V - V_P}{R_1} = \frac{V - \frac{VR}{R_1}}{R_1}$$

$$\therefore R_{in} = \frac{V}{I} = \frac{R_1}{1-\frac{R}{R_1}}$$

43. Ans: (b)

Sol: Conversion time $t_A = 10\mu s$

Sampling frequency $f_{s(max)} = \frac{1}{t_A} = \frac{1}{10\mu s}$

$= 0.1$ MHz $= 100$ kHz

$f_{s(max)} = 2f_{m(max)}$

Maximum input signal frequency

$$f_{m(max)} = \frac{f_{s(max)}}{2} = \frac{100kHz}{2} = 50kHz$$

44. Ans: (c)

Sol: Bus idle machine cycles are required for the execution of DAD and TRAP interrupt.

45. Ans: (a)

Sol: Let number of Flip-flops required be N.

$2^N \geq 6000$

N = 13

46. Ans: (a)

Sol: No flags will be affected when data transfer instructions are executed.

47. Ans: (c)

Sol: In this $J_A = \overline{B}+\overline{C}, K_A = BC, J_B = A,$

$K_B = \overline{A}, J_C = B, K_C = \overline{B}$

CLK	J_A K_A	J_B K_B	J_C K_{C}	A B C
0				0 0 0
1	1 0	0 1	0 1	1 0 0
2	1 0	1 0	0 1	1 1 0
3	1 0	1 0	1 0	1 1 1
4	0 1	1 0	1 0	0 1 1
5	0 1	0 1	1 0	0 0 1
6	1 0	0 1	0 1	1 0 0

0, 4, 6, 7, 3, 1, 4,…..

Hence, modulus of the counter is 5

48. Ans: (a)

Sol: $x_2 = b_2 \oplus b_1 \oplus b_1 = b_2 \oplus 0 = b_2$

$x_1 = b_2 \oplus b_1$

$x_0 = b_0 \oplus b_1$

b_2	b_1	b_0	x_2	x_1	x_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0

i.e., binary to gray code converter

49. Ans: (d)

Sol:

ADC	Conversion time
Counter type ADC	$(2^n-1)T_{CLK}$
Flash type ADC	$1.T_{CLK}$
Successive Approx. ADC	$N.T_{CLK}$
Dual Slope ADC	$2^{n+1}.T_{CLK}$

So, Dual Slope ADC has maximum conversion time.

50. Ans: (c)

Sol:

```
       MVI  C, 0A H = 7T
       XRA  A       = 4T
LOOP:  DCR  C       = 4T
       INC  A       = 4T
       JNZ  LOOP    = 7T/10T
```

So,

Number of T states required

= 7T + 4T + (09 × 18) T + 4T + 4T + 7T

= 7T + 4T + 162T + 4T + 4T + 7T = 188T

51. Ans: (d)

Sol: $\sqrt{224_r} = 13_r \Rightarrow \left(\sqrt{2r^2+2r+4}\right)_{10} = (r+3)_{10}$

$\Rightarrow 2r^2+2r+4 = r^2+6r+9$

$\Rightarrow r^2-4r-5=0 \Rightarrow r^2-5r+r-5=0$

$r(r-5)+1(r-5)=0$

$(r+1)(r-5)=0$

i.e. Radix r = 5

52. Ans: (b)

Sol: For odd number of 1's at the input, the sequential circuit remains in 'S_1' state producing the output 1.

53. Ans: (d)

Sol: $f(x,y,z) = \sum (m_0, m_2, m_7) = \sum m(0, 2, 7)$

$f'(x,y,z) = \sum (m_1, m_3, m_4, m_5, m_6)$

$= \Pi (M_0, M_2, M_7)$

54. Ans: (d)

Sol: size = $2^x \times y \times n$

Let n be the number of chips.;

$x \rightarrow$ no. of address lines

$y \rightarrow$ no. of data lines

$2^x \times y \times n = 32$ KB

$2^{12} \times 4 \times n = 32 \times 1024 \times 8$

$$n = \frac{32 \times 1024 \times 8}{2^{12} \times 4} = 16$$

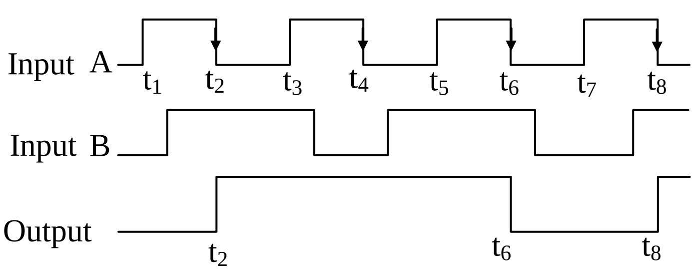
n = 16

55. Ans: (b)

Sol: XOR gate, Half adder, Full subtractor are combinational circuits, register is a sequential circuit.

56. Ans: (c)

Sol: A is connected as negative edge clock input for T-flip-flop. So, for every negative edge B is applied to FF. $Q(t+1) = T \oplus Q(t)$



57. Ans: (b)

Sol: If A = 1, then irrespective of 'B' output is '0'. Since transistors are ON

If A = 0, then transistors are OFF &

If B = 0, diode ON $\Rightarrow Y_0 = 0$

If B = 1, diode OFF $\Rightarrow Y_0 = 1$

A	B	Y_0
1	0	0
1	1	0
0	0	0
0	1	1

$\Rightarrow Y_0 = \overline{A}B$

58. Ans: (a)

Sol: F(A,B,C,D)

$= \overline{A}B\overline{D}.C + A\overline{B}\,\overline{D}.1 + \overline{A}BD.1 + A\overline{B}D.\overline{C}$

$= \overline{A}BC\overline{D} + A\overline{B}\,\overline{D} + \overline{A}BD + A\overline{B}\,\overline{C}D$

$= \overline{A}B(C\overline{D} + D) + A\overline{B}(\overline{D} + \overline{C}D)$

$= \overline{A}B(C + D) + A\overline{B}(\overline{C} + \overline{D})$

59. Ans: (b)

Sol: A n-bit shift register requires n flip-flops.

A n-bit ripple counter requires n flip-flops.

A n-bit synchronous counter requires n flip-flops.

A n-bit ring counter requires n flip-flops.

60. Ans: (c)

Sol: $F = (B\overline{C} + \overline{A}D)(A\overline{B} + C\overline{D})$

$F = B\overline{C}A\overline{B} + B\overline{C}C\overline{D} + \overline{A}DA\overline{B} + \overline{A}DC\overline{D}$

$F = 0$

$\overline{F} = 1$

Number of literals in $\overline{F} = 1$ is 0.

61. Ans: (d)

Sol: (A) 8255-PPI

(B) 8257-DMAC

(C) 8251-USART

(D) 8254-TIMER

(E) 8259-PIC

62. Ans: (a)

Sol: $F(A, B, C) = AB + \bar{A}C + BC$

$= AB(C+\bar{C}) + \bar{A}(B+\bar{B})C + (A+\bar{A})BC$

$= ABC + AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}C + ABC + \bar{A}BC$

A \ BC	00	01	11	10
0		1	1	
1			1	1

$\bar{A}C$ – EPI

BC – Non EPI

AB – EPI

63. Ans: (c)

Sol:

MVI A, 45H	: $A \leftarrow 45H$
MOV B, A	: $B \leftarrow A$; A = B = 45H
STC	: CY = 1
CMC	: CY = 0
RAR	: A = 22H ; CY = 1
XRAB	: $A \oplus B = 22H \oplus 45H = 67H$
HLT	: Halted

64. Ans: (c)

Sol: $(23E)_X = 2X^2+3X+E$

In the given number 'E' is the highest digit so we can take its radix from greater than equal to F. So,

$= 2(15)^2 + 3(15)^1 + E(15)^0$

$= 2(225) + 3(15) + 14 = 509$

65. Ans: (a)

Sol: For the given circuit to function as an oscillator the number of inverters N should be odd.

$$f_{osc} = \frac{1}{2Nt_{pd}}$$

$t_{pd} = 10$ n sec

$$f_{osc} = \frac{1}{2\times(10\,\text{n sec})\times N}$$

$$= \frac{10^8}{2\times1\times N} = \frac{10^2\times10^6}{2N} = \frac{50}{N}\text{MHz}$$

66. Ans: (c)

Sol: Adding two n-bit numbers,

ROM inputs = n+n = 2n

Adding two n-bit numbers largest result size = (n+1) bits

$\therefore$ ROM size = $2^{2n} \times (n+1)$ bits

67. Ans: (c)

Sol: ROM, Hard disk & Magnetic disk are Non-Volatile

RAM is Volatile

68. Ans: (c)

Sol: Given, N = 10 and Input-Range = (0 – 20)V

For proper operation of ADC,

Ripple voltage < Resolution of ADC

$$\text{Resolution of ADC} = \frac{\text{Input voltage Range}}{2^N - 1}$$

$$= \frac{20}{2^{10}-1} \cong 20\text{mV}$$

69. Ans: (c)

Sol: $\rightarrow$ The 8051 microcontroller is a 8-bit processor and it is based on Harvard architecture.

70. Ans: (c)

Sol: Transfer function applicable for only linear time invariant systems.

71. Ans: (a)

Sol: $$\text{T.F} = \frac{40}{(s+2)(s+20)}$$

DC gain should not change after removing far pole.

DC gain before removing far pole

$$= \frac{40}{(0+2)(0+20)} = 1$$

$$\text{T.F after removing far pole} = \frac{K}{s+2}$$

$$\text{DC gain} = \frac{K}{0+2} = \frac{K}{2}$$

$\therefore \dfrac{K}{2} = 1 \Rightarrow K = 2$

$T.F = \dfrac{2}{s+2}$

Comparing with standard 1st order T.F $\dfrac{A}{s+T}$

$\therefore$ Time constant $= \dfrac{1}{T} = \dfrac{1}{2}$

2% Settling time, $t_s = 4\times\dfrac{1}{2} = 2$ sec which depends on dominant pole.

72. Ans: (d)

Sol: A fixed bias BJT circuit cannot exhibit better performance as compared to self bias BJT circuit. Hence **Statement (I)** is false.

73. Ans: (c)

Sol: All Software interrupts of 8085 are Maskable and Vectored. So, Statement (I) is true.

Software interrupts are not random in nature. So, Statement (II) is false.

74. Ans: (b)

Sol: Any Boolean function can be realized by using a suitable multiplexer.

So, statement (I) is true.

A multiplexer can be realized using NAND and NOR gates, which are universal gates. So, statement (II) is true

Statement (I) and Statement (II) are individually true but Statement (II) is not correct explanation for Statement (I).

75. Ans: (a)

Sol: Tri-state logic has three states i.e. logic high, logic low, high impedance.

Tri-state logic is used when more than one input/output devices connected to the same data bus in a digital system by helping in isolating the input/output devices from the data bus.