TEST ID: 201

ACE
Engineering Academy

Head Office : Sree Sindhi Guru Sangat Sabha Association, # 4-1-1236/1/A, King Koti, Abids, Hyderabad - 500001.
Ph: 040-23234418, 040-2324419, 040-2324420, 040-24750437

Hyderabad | Kukatpally | Kothapet | Delhi | Bhopal | Patna | Pune | Bhubaneswar | Lucknow | Bengaluru | Chennai | Vijayawada | Vizag | Tirupati | Kolkata | Ahmedabad

ESE- 2020 (Prelims) - Offline Test Series Test- 1

ELECTRICAL ENGINEERING

SUBJECT: ANALOG, DIGITAL ELECTRONICS AND BASIC ELECTRONICS ENGINEERING - SOLUTIONS

01. Ans: (d)

Sol: $V_{rms} = \frac{V_m}{\sqrt{2}}$

$V_m = \sqrt{2}\, V_{rms} = 50\sqrt{2}$ volts

PIV of diode in centre tapped is $2V_m$

$PIV = 2 \times 50 \times \sqrt{2}$

$= 100\sqrt{2}$ volts

$= 141.4V$

02. Ans: (c)

Sol: For +ve cycle, D_1 is forward biased.

C_1 starts charging.

C_1 charges till 1V.

For –ve cycle, D_2 is forward biased.

$V_C = -V_i - (-1) = -(-1) + 1 = 2V$

03. Ans: (c)

Sol: $A_I = \frac{h_{fe}}{\sqrt{1+\left(f/f_\beta\right)^2}}$, $f_\beta = \frac{1}{2\pi r_\pi \left(C_\pi + C_\mu\right)}$

Current gain of BJT drops at high frequency due to junction capacitor

04. Ans: (a)

Sol: $V_E = 0$, $V_C = 0.2V$

$I_C = \frac{10 - 0.2}{2k} = 4.9mA$

To operate transistor remain in saturation is

$I_B > \frac{I_C}{\beta}$

$\frac{V_i - 0.7 - 2 - 0.7}{5k} > \frac{4.9 \times 10^{-3}}{50}$

$(V_i - 3.4) > 0.49$

$V_i > 3.89V$

05. Ans: (c)

Sol: $I_C = 1.3mA$

$r_e = \frac{V_T}{I_C} = \frac{26mV}{1.3mA} = 20\Omega$,

$A_v = -\frac{R_L}{r_e}$, $R_L = 2k \,||\, 2k = 1k\Omega$

$A_v = -\frac{1000}{20}$

$A_v = -50$

06. Ans: (c)

Sol: Increasing order of input impedance

(1) CB (Common base)

(2) CE (Common emitter)

(3) CC (common collector or emitter follower / Buffer)

(4) Emitter follower using darlington pair

07. Ans: (d)

Sol: $A_v = A_{v1} \,.\, A_{v2}$

$= 200 \times 500 = 10^5$

$(A_v)_{dB} = 20\log_{10}(10^5)$

$= 100$

08. Ans: (a)

Sol: Due to voltage series feedback, input resistance increased by the factor of $(1 + A\beta)$

$\Rightarrow Z_{IF} = Z_i (1 + A\beta)$

$$Z_{IF} = 2 \times 10^3 \left(1 + \frac{4}{100} \times 100\right)$$

$Z_{IF} = 10k\Omega$

09. Ans: (c)

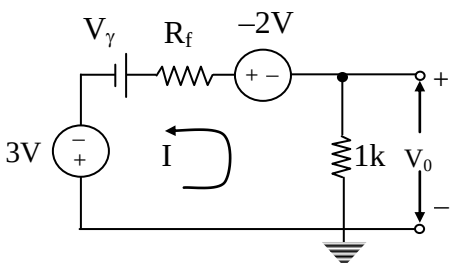
Sol: In the circuit shown Voltage sampling (output) & Current mixing (input). So it is a trans-resistance Amplifier.

10. Ans: (a)

Sol: : Emitter follower (CC amplifier), (voltage series amplifier)
: It acts as Buffer amplifier
: Good impedance matching
: High input impedance
: Low output impedance
: $A_v \simeq 1$
: A_I (current gain) is high
: Power gain = current gain

11. Ans: (c)

Sol: $(V_A - V_c)$ of diode is 1V
Diode is ON state



$$I = \frac{-2 - 0.6 + 3}{1100}$$

$$= \frac{0.4}{1100} = 0.36mA$$

$$\Rightarrow V_0 = -0.36mA \times 10^3$$

$$V_0 = -0.36V$$

12. Ans: (d)

Sol: Since base and collector are short circuited the transistor will act as a diode and hence diode equation is used.

$$I_E \approx I_0 . e^{V_D / V_T}$$

$$\Rightarrow V_D = V_X = V_T \ \ell n\left(\frac{I_E}{I_0}\right)$$

$$= 26 \times 10^{-3} \ell n\left(\frac{3 \times 10^{-3}}{10^{-9}}\right)$$

$= 26 \times 10^{-3} \ \ell n\ (3 \times 10^6)$
$= 26 \times 10^{-3} [\ell n\ 3 + \ell n\ 10^6)$
$= 26 \times 10^{-3}\ [1.1 + 2.3 \times 6]$
$= 26 \times 10^{-3} (14.9)$

$V_X = 0.39V$

13. Ans: (c)

Sol: Gain of Amplifier $= -\frac{R_2}{R_1}$

Feedback factor is $\beta = \frac{-L_1}{L_2}$

Condition for oscillation is $A\beta = 1$

$$\left(-\frac{R_2}{R_1}\right)\left(\frac{-L_1}{L_2}\right) = 1$$

$$\frac{-R_2}{R_1} = \frac{-L_2}{L_1} \Rightarrow \frac{L_1}{R_1} = \frac{L_2}{R_2}$$

14. Ans: (d)

Sol: The bias stability of an Emitter-Bias Amplifier circuit improves by decreasing the value of R_B and increasing the value of R_E.

15. Ans: (a)

Sol: Wien bridge oscillator generates Audio frequency range oscillations.
Crystal oscillator generates RF frequency range oscillations.
The output impedance of Voltage shunt feedback amplifier is low.
The output impedance of Current shunt feedback amplifier is high.

SSC-JE (Paper-II) MAINS 2018

OFFLINE TEST SERIES

Streams: Civil | Electrical | Mechanical

FULL LENGTH MOCK TEST-1

Exam Date: **01.12.2019**

Exam Timing: **6:00 pm to 8:00 pm**

FULL LENGTH MOCK TEST-2

Exam Date: **15.12.2019**

Exam Timing: **6:00 pm to 8:00 pm**

- All tests will be conducted in **Question Paper Booklet** format.
- Test Series will be conducted at all our centres.

Hyderabad | Delhi | Pune | Bhubaneswar | Bengaluru | Chennai | Vijayawada | Vizag | Tirupathi | Kukatpally | Kolkata | Ahmedabad

040 - 48539866 / 040 - 40136222 testseries@aceenggacademy.com

ISRO

इसरो ISRO

ONLINE TEST SERIES

No. of Tests : 15

Subject Wise Tests : 12 | Mock Tests : 3

Indian Space Research Organisation (ISRO)
Recruitment of Scientist/Engineer 'SC'

ELECTRONICS | MECHANICAL | COMPUTER SCIENCE

Starts from 5th November 2019

All tests will be available till 12-01-2020.

040 - 48539866 / 040 - 40136222 testseries@aceenggacademy.com

16. Ans: (b)

Sol: For a rectifier with inductor filter, ripple factor $\gamma \alpha R_L$ for 'γ' to be low, load of less resistance should be selected and hence a rectifier with 'L' filter is more suitable for high load current.

$\rightarrow$ similarly, for a rectifier with 'C' filter.

$$\gamma \alpha \frac{1}{R_L}$$

$\therefore$ This filter is suitable for low load currents

$\rightarrow$ For LC filter, 'γ' independent of load.

17. Ans:(d)

Sol: In an RC coupled amplifier, the external capacitors establish the lower 3-dB frequency and the device junction capacitors are responsible for upper 3-dB frequency.

Case (i): As the amplifier is an RC coupled circuit, the coupling capacitors will establish the lower 3-dB frequency $\left(f_L = \frac{1}{2\pi R_i C_B} \text{ or } f_L = \frac{1}{2\pi R_L C_C} \right)$.

Case (ii): If the device junction capacitors are open for the frequency range of input signal, the gain of the amplifier is constant from mid-frequencies to high frequencies.

18. Ans: (a)

Sol: The main difference between BJT and MOSFET is current is quadratic with V_{GS} for MOSFET and exponential with V_{BE} for BJT.

In MOSFET,

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})]^2$$

In BJT, $I_C = I_0[e^{V_{BE}/\eta V_T} - 1]$

19. Ans: (b)

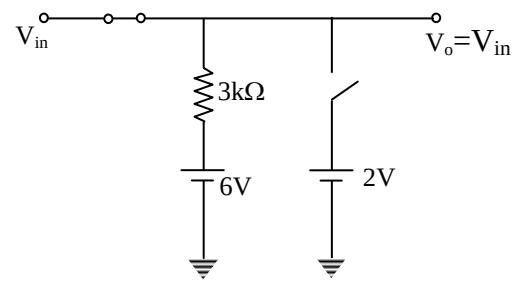
Sol: Hysteresis in a comparator makes immune to false triggering caused by noisy input signal.

20. Ans: (d)

Sol: Given circuit is integrator circuit. If square wave is applied to integrator, it produces triangular waveform.

21. Ans: (d)

Sol:

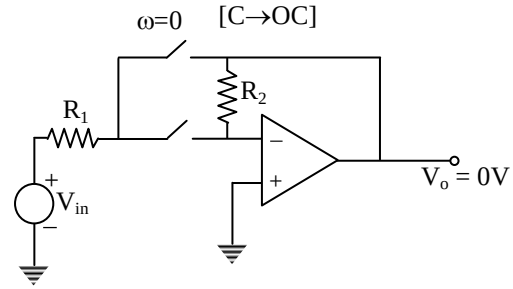


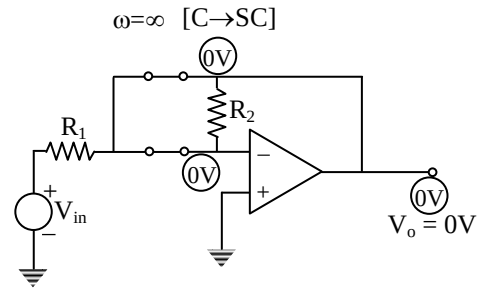
D_2 is always RB

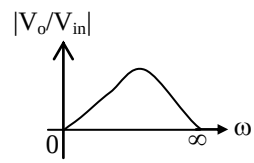
$V_{in} > 6V$ (D_1 FB)

22. Ans: (c)

Sol:







23. Ans: (b)

Sol: A_v in dB = $20\log_{10} A_v$ = 80 dB

$\Rightarrow A_v = 10^4$

Bandwidth f_H = 30 Hz

Gain-Bandwidth product = $10^4 \times 30$ Hz

= 300 kHz

24. Ans: (a)

Sol: For start input $\rightarrow$ J = 1, K = 0 $\rightarrow$ Then Q becomes 1.

CLK	Counter Output	J	K	Q
0	000(0)	1	0	1
1	001(0)	0	0	1
2	010(0)	0	0	1
3	011(0)	0	0	1
4	100(0)	0	0	1
5	101(0)	0	0	1
6	110(0)	0	0	1
7	111(1)	0	1	1
8	-	-	-	0

K Input becomes 1 after 7^{th} clock pulse

[$\because Q_2 Q_1 Q_0 = 111$]

Thus output is cleared i.e., Q is 0 after 8^{th} clock pulse

$$\text{width of pulse} = 8T = \frac{8}{f} = \frac{8}{5\text{MHz}} = 1.6\mu s$$

25. Ans: (a)

Sol: Given 2 numbers 1011 and 0110

1011 is in 2's complement form. Its decimal representation is $(-5)_{10}$

0110 is in true binary form. Its decimal representation is $(6)_{10}$

Its addition results $(+1)_{10} = (0001)_2$

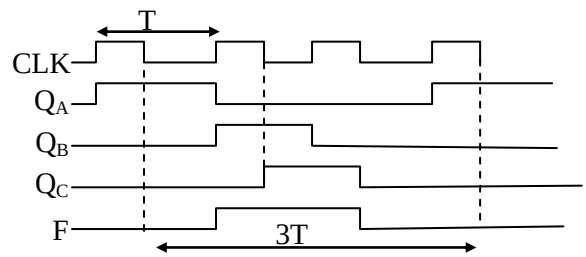
26. Ans: (b)

Sol: ALE (Address Latch Enable) signal is used for differentiating AD_7 to AD_0 multiplexed data, whether it is address or data.

27. Ans: (b)

Sol: $D_A = \overline{Q_A}.\overline{Q_B}$, $D_B = Q_A$, $D_C = Q_B$

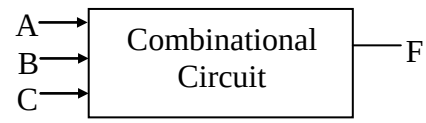
D_A	D_B	D_C	Q_A	Q_B	Q_C
			0	0	0
1	0	0	1	0	0
0	1	1	0	1	1
0	0	0	0	0	0



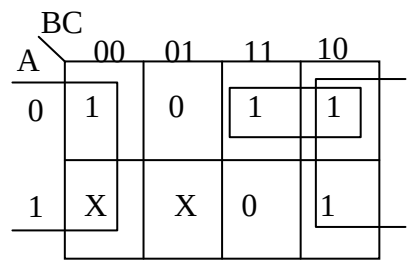
So, it is a Divide by 3 circuit, with 50%, Duty cycle.

28. Ans: (a)

Sol:



$F(A,B,C) = \sum m(0,2,3,6) + d(4,5)$



$F = \overline{C} + \overline{A}B$

$F = \overline{\overline{F}} = \overline{C \quad \overline{\overline{A}.B}}$

So, 2 number of two input NAND gates are required.

29. Ans: (a)

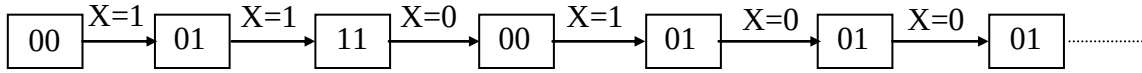
Sol: Given $D_A = X.B$

$D_B = \overline{A}$

P.S A	B	Input X	FF Inputs D_A	D_B	N.S A	B	Output Y
0	0	0	0	1	0	1	0
0	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	1

The value of X at –ve edges of all clock pulses are 1, 1, 0, 1, 0, 0, 0

Thus the state transitions are



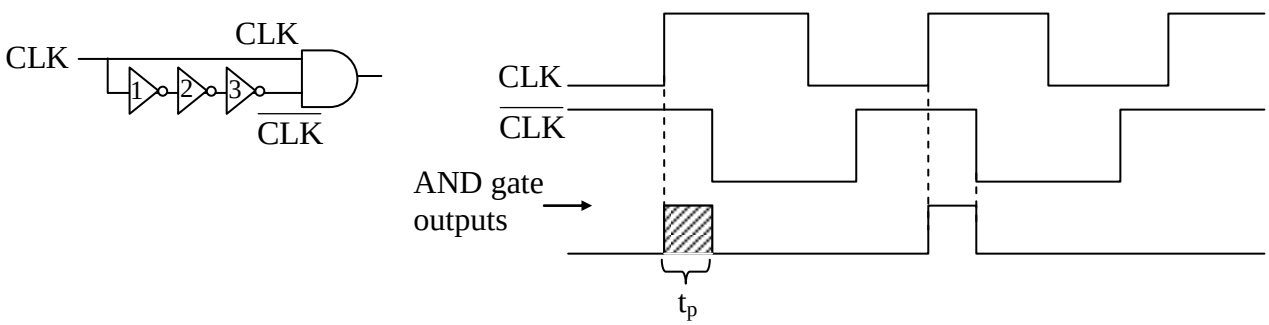
Output

Y 0 0 1 0 0 0 0 [$\because$ Output Y = A.B]

Number of times output is high equals to 1.

30. Ans: (c)

Sol:



$t_p \le 15$ ns to avoid Race around condition ($t_p < t_{FF} < T$)

i.e., t_p , max = 15 ns which is equal to 3 inverters propagation delay

$3\ t_{pi} = 15$ns

$t_{pi} = 5$ns

TEST YOUR PREP

IN A REAL TEST ENVIRONMENT

Pre GATE - 2020

Date of Exam : **18th January 2020**
Last Date to Apply : **31st December 2019**

Highlights:

- Get real-time experience of **GATE-20** test pattern and environment.
- Virtual calculator will be enabled.
- Post exam learning analytics and All India Rank will be provided.
- Post **GATE** guidance sessions by experts.
- Encouraging awards for **GATE-20** toppers.

PAN INDIA
PRESENCE AVAILABLE IN MORE THAN
30 CITIES

SSC-JE (Paper-I)

Online Test Series

Staff Selection Commission - Junior Engineer

No. of Tests : 20

Subject Wise Tests : 16 | Mock Tests - 4

Civil | Electrical | Mechanical

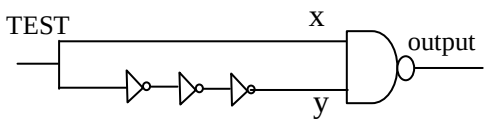
AVAILABLE NOW

All tests will be available till **SSC 2019 Examination**

040 - 48539866 / 040 - 40136222 testseries@aceenggacademy.com

31. Ans: (d)

Sol:



Initially when test input is low output is high (assume identical non zero delay)

When test becomes high:-

x = high, y remains high till the 3 NOT gate combination, make the input logic low. So, Output goes to low. After some delay Y becomes logic low. Then output becomes high.

So, output switches from high to low to high and remains high.

Option (d) is correct.

32. Ans: (d)

Sol: From state diagram x-FF Truth table is

x	Q(t + 1)
0	$\overline{Q(t)}$
1	Q(t)

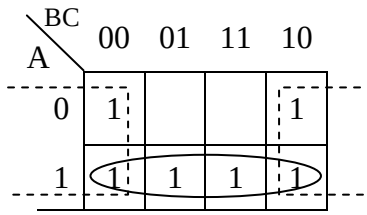
$\Rightarrow$

x	Q(t)	Q(t + 1)
0	0	1
0	1	0
1	0	0
1	1	1

i.e., $Q(t+1) = \overline{x \oplus Q(t)}$

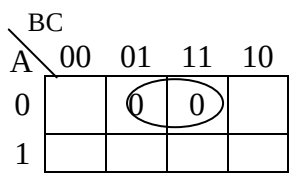
33. Ans: (b)

Sol:



$A + \overline{C}$

(OR)



$A + \overline{C}$

34. Ans: (a)

Sol: Delay of a k-bit Carry-Lookahead Adder

$T_{lookahead-adder} = 4\,[\log_4 k]$

k	$T_{lookahead-adder}$
4	4
16	8
32	12
64	12
128	16
256	16

Delay in Carry Look Adder

$T_{CLK} = 4 \log_4 K$

$T_{CLK} = 4 \log_4 128$

$= 16$

35. Ans: (c)

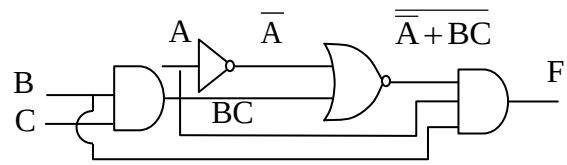
Sol: let us assume two numbers as 1011 and 111, then its multiplication is

$$\begin{array}{r} 1011 \\ \times\ 111 \\ \hline 1011 \\ 1011 \\ 1011 \\ \hline 1001101 \end{array}$$

So, we require two number of 4-bit binary adders.

36. Ans: (b)

Sol:



$F = A.B\left(\overline{\overline{A} + BC}\right)$

$F = AB\overline{C}$

37. Ans: (a)

Sol: $F = \left(\overline{A}\,\overline{D} + B\overline{D}\right)\left(A + B + D\right)$

$F = \overline{A}B\overline{D} + AB\overline{D} + B\overline{D}$

$= B\overline{D}\left[\overline{A} + A + 1\right]$

$F = B\overline{D}$

38. Ans: (d)

Sol: $V_{FS} = 5V$

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{5V}{2^{10} - 1} = 0.00488V$$

$$= 4.88mV$$

39. Ans: (a)

Sol: $J_A = BC,\ K_A = \overline{B},\ J_C = K_C = \overline{A}$

and B Toggles when C changes from 1 to 0

PS	FF Inputs	NS
A B C	$J_A K_A$ $J_C K_C$	A B C
1 0 1	0 1 0 0	0 0 1

40. Ans: (c)

Sol: RST n $\Rightarrow$ n × 8 $\Rightarrow (n \times 8)_{10} \Rightarrow$ XXXXH

RST 4.5 $\Rightarrow 4.5 \times 8 = (36)_{10} \Rightarrow$ 0024H

41. Ans: (c)

Sol: Let us take A is loaded is 53H, so when XRA A is executed EXOR operation is performed,

$$\begin{array}{r} 01010011 \\ (+)\ \underline{01010011} \\ 00000000 \end{array} \qquad \begin{array}{l} \text{XRA A} \rightarrow A \oplus A \\ = 0 \end{array}$$

This means result is 00H, CY = 0 and Z = 1

42. Ans: (a)

Sol: To get the physical address, the contents of segment register are multiplied by 16 i.e., shifted by 4 positions to the left by inserting 4 zero bits and then the offset i.e., contents of pointer register are added to the contents of SS.

Physical address = 40000H + 9F20H

= 49F20H

43. Ans: (b)

Sol:

$$\begin{array}{r} A = 37H = 0011\ \ 0111 \\ 56H = \underline{0101\ \ 0110} \\ 1000\ \ 1101 \\ \underline{\qquad\qquad +1} \text{ - carry generated from previous executions} \\ 1000\ \ 1110 = 8EH \end{array}$$

44. Ans: (c)

Sol:
- → flip-flop is used to store 1-bit of information.
- → Race-around condition occurs in J-K flip-flop when both the inputs are 1.
- → A transparent latch consists of D type flip-flop.
- → Master-slave configuration is used to prevent race around condition.

45. Ans: (c)

Sol: LXI H,4000H -Immediate Addressing mode
RNZ - Implicit Addressing mode
XRA B - Register Addressing mode
LDA 1560H - Direct Addressing mode

46. Ans: (d)

Sol: Conversion time of Successive Approximation ADC is nT

$$T_A = nT_{clk} = 5 \times \frac{1}{10M} = 0.5\mu s$$

$f_s \rightarrow$ Sampling frequency

$f_m \rightarrow$ Input signal frequency

$$f_{s(max)} = \frac{1}{0.5\mu s} = 2MHz$$

$$f_{s(max)} = 2f_{m(max)}$$

$$f_{m(max)} = \frac{f_{s(max)}}{2} = \frac{2MHz}{2} = 1MHz$$

47. Ans: (a)

Sol: Step size $\Delta = \frac{V_{max} - V_{min}}{2^n} = \frac{10V - 0V}{2^{10}}$

maximum possible error

$= \frac{\Delta}{2} = \frac{10V}{2^{11}} = 0.00488V = 4.88mV$

48. Ans: (c)

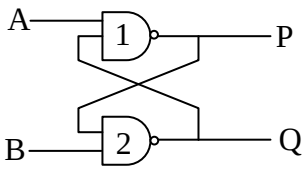
Sol: $V_0 = -V_R\left(\frac{R_F}{R}\right)\left(d_1 2^{-1} + d_2 2^{-2} + ...d_n 2^{-n}\right)$

$V_0 = -8V\left(\frac{10k}{10k}\right)\left(\frac{1}{2} + 0 + \frac{1}{2^3}\right) = -5V$

49. Ans: (c)

Sol:

A	B	P	Q
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	No Change	



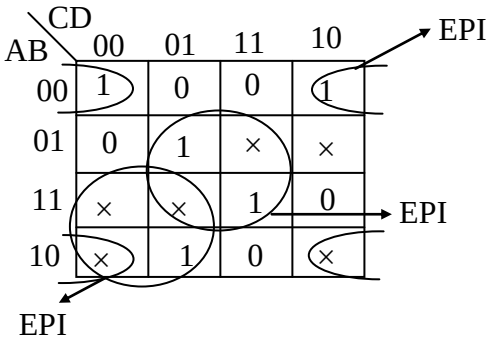
When A = 1, B = 0

$\Rightarrow$ P = 0, Q = 1

50. Ans: (c)

Sol: EPI is a PI which contains at least one '1' which can't be covered by any other PI is called EPI.

The K map for F(A, B, C, D) is



So, 3 EPI's

51. Ans: (d)

Sol: Base - 6 number of system

The numbers present are

$0 \rightarrow 000$

$1 \rightarrow 001$

$2 \rightarrow 010$

$3 \rightarrow 101$

$4 \rightarrow 110$

$5 \rightarrow 111$

As the code is given to be self complementary, code of 0 & 5 are complementary to each other.

Similarly the code of 1 & 4 are complementary to each other.

$\therefore$ Code of 4 = 110

52. Ans: (d)

Sol: f(A, B, C) = Σm(0, 2, 6, 7) in SOP form

$= \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + AB\overline{C} + ABC$

Its complement = $\bar{f}(A,B,C)$

$= \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}\,\overline{C} + A\overline{B}C$

53. Ans: (b)

Sol: Image frequency, $f_i = f_s + 2IF$

where IF (intermediate frequency) = 10.7 MHz, f_s = 90.6MHz

f_i = 90.6 + 21.4 = 112 MHz

54. Ans: (c)

Sol: $\mu = 1$ given

$P_t = P_C\left[1 + \frac{\mu^2}{2}\right]$

$\Rightarrow P_t = \frac{3}{2}P_C = 1.5P_C$

55. Ans: (b)

Sol: Bandwidth of FM = $2(\beta + 1)f_m$

For WBFM $\beta >> 1$. So, Bandwidth $\approx 2\beta f_m$

$\beta = \frac{BW}{2f_m}$

f_m is constant. As transmission bandwidth increases, β also increases proportionally.

Thus if bandwidth is doubled β also gets doubled.
But figure of merit of FM

$$FOM = \frac{SNR_{O/P}}{SNR_{I/P}} = \frac{3}{2}\beta^2$$

Thus when β is doubled FOM increases four fold.

56. Ans: (b)

Sol: An Envelope detector is a diode half wave rectifier followed by an RC-low pass detector. The output of the detector represents the envelope of the incoming high frequency signal. It is used for FSK signals.
Envelope detector is also called as non synchronous detector since local oscillatory circuit is not implemented in detection.

57. Ans: (d)

Sol: RF amplifier is used to improve the rejection of the image frequency.

58. Ans: (b)

Sol: Bandwidth

$$= \frac{1}{2} \times \text{sampling rate} \times \text{Number of unit code}$$

$$= \frac{1}{2} \times 10k \times 7$$

= 35 kHz

59. Ans: (c)

Sol: The use of non-uniform quantizer leads to the increase in SNR for low level signals.

60. Ans: (b)

Sol:

- The bandwidth of the AM depends on the bandwidth of the modulating system
  i.e B.W = $2f_m$.
- The bandwidth of the AM cannot depend on the modulation index.
- Practically FM bandwidth depends upon percentage of modulation index.

61. Ans: (d)

Sol: $m(t)_{max} = 1$

$f_i = f_c + k_f\, m(t)$ = 1MHz + 1kHz /V × V
= 1.001 MHz

62. Ans: (d)

Sol: $V_T = \frac{\sqrt{2qN_A \in_S (2\phi_B)}}{C_{OX}} + 2\phi_B + V_{FB}$,

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Threshold voltage can be decreased by decreasing the channel dopant concentration and reducing the gate-oxide thickness and decreasing source to body voltage. So, option (d) is correct.

63. Ans: (d)

Sol: Darlington amplifier: High input impedance & low output impedance
Differential amplifier: CMRR is very high
Cascode amplifier (FET): Low input capacitance but high R_{in}.
Common gate amplifier: Low input impedance & high output impedance.

64. Ans: (c)

Sol: Since, drain and gate are shorted, the MOSFET operates in saturation region

$$\frac{I_{D2}}{I_{D1}} = \frac{(V_{GS2} - V_T)^2}{(V_{GS1} - V_T)^2} = \frac{(4V - 1V)^2}{(3V - 1V)^2}$$

$$\Rightarrow I_{D2} = \frac{9}{4} I_{D1} = 9mA$$

65. Ans: (b)

Sol: Gallium Arsenide phosphide (GaAsP) is a direct band gap semiconductor and hence is used in LEDs.

66. Ans: (a)

Sol: (i) Intrinsic semiconductors have negative temperature co-efficient. Therefore conductivity of germanium increases by 6% per °C rise in temperature.

ACE Engineering Academy

HEARTY CONGRATULATIONS TO OUR ESE - 2019 TOP RANKERS

TOTAL SELECTIONS in Top 10: 33

(EE: 9, E&T: 8, ME: 9, CE: 7) and many more...

ACE

DIGITAL CLASSES

for

ESE 2020/2021
General Studies &
Engineering Aptitude

GATE 2020/2021
Computer Science &
Information Technology

Access the Course at

www.deep-learn.in

(ii) The conductivity of silicon increases by 8% per °C rise in temperature.

(iii) Metals have positive temperature coefficient, so the resistance of metals increases by 0.4% per °C rise in temperature.

67. Ans: (b)

Sol: With negative gate to source ($-V_{GS}$) voltage an n-channel JFET operated as an amplifier. So, gate-source junction should be reverse biased.

68. Ans: (c)

Sol: $I_{D1} = I_{D2}$

$\Rightarrow K_1[V_{GS1} - V_T]^2 = K_2[V_{GS2} - V_T]^2$

$\sqrt{\frac{K_1}{K_2}}[V_{GS1} - V_T] = V_{GS2} - V_T$

$2[5 - V_o - 1] = V_o - 1$

$\Rightarrow 2(4 - V_o) = V_o - 1$

$\Rightarrow V_o = 3\text{Volts}$

69. Ans: (c)

Sol: $r_o = \frac{1}{\lambda . I_D} = \frac{1}{0.05V^{-1} \times 1 \times 10^{-3} A} = 20k\Omega$

70. Ans: (b)

Sol: Zener diode is a breakdown diode, it has to be operated in reverse bias to produce breakdown.

Solar cell produces current when carriers are generated by solar power so solar cell is forward biased.

LED & LASER are light emitting diodes with direct recombination of majority concentration of carrier must be forward biased.

Photo diodes must be producing photo conduction possible only in reverse bias.

71. Ans: (d)

Sol: Beyond Critical Wavelength, photo electric emission can not take place.

72. Ans: (a)

Sol: In a CE amplifier if the bypass capacitor is open, the unbypassed emitter resistor provides

negative feedback and will reduce the voltage gain and increase the input resistance.

73. Ans: (a)

Sol: Slew Rate (SR) = $\left.\frac{dV_0}{dt}\right|_{max}$

In ideal Op-Amp Slew Rate is very high.

74. Ans: (b)

Sol: Master slave JK Flip Flop suffers from ones catching problem. So, statement I is true.

Negative Edge Triggered Flip Flop ignores the pulses that occur when clock pulse is high. So, statement II is true. But Statement II is not correct explanation for statement I.

75. Ans: (d)

Sol: FM has better noise performance than AM. So, statement I is false.

In WBFM the number of signal components decided by the modulation index β.

As β increases signal strength increases but this is not the case in AM. The drawback is as we increase β in WBFM, the corresponding bandwidth also increases. So, in WBFM always the trade off present between bandwidth and SNR.