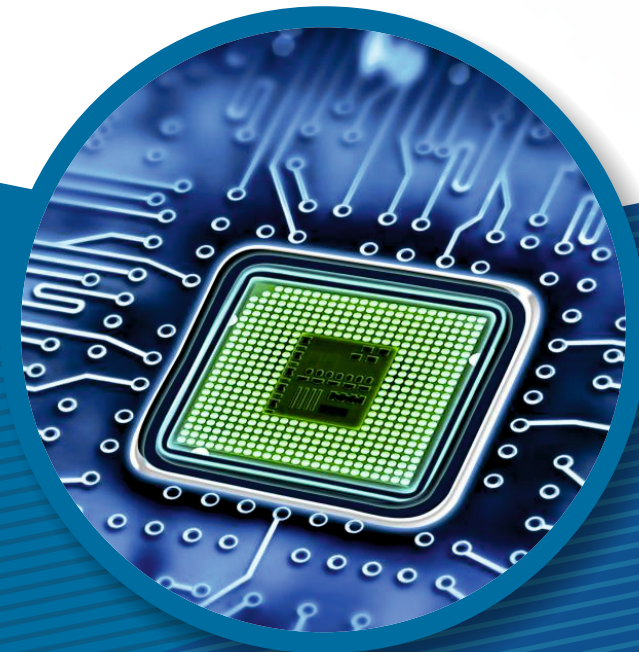




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**ELECTRONICS &
TELECOMMUNICATION
ENGINEERING**

ELECTRONIC DEVICES & VLSI

Text Book : Theory with worked out Examples
and Practice Questions

Chapter 1 Basics of Semiconductor

(Solutions for Text Book Practice Questions)

Objective Practice Solutions

01. Ans: (a)

Sol: $N_D = 5 \times 10^{22} \times \frac{1}{10^9} \text{ cm}^{-3}$
 $= 5 \times 10^{13} \text{ cm}^{-3}$

According to mass action law

$$np = n_i^2$$

$$n_n p_n = n_i^2$$

$$N_D p_n = n_i^2 \quad (\because n_n \approx N_D)$$

$$p_n = \frac{n_i^2}{N_D}$$

$$p_n = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{13}}$$

$$= 4.5 \times 10^6 \text{ cm}^{-3}$$

02. Ans: (b)

Sol: According to law of mass action $n.p = n_i^2$

Where n_i = intrinsic carrier concentration.

N_D = doping concentration for a n-type material.

Majority carrier concentration

$$n \approx N_D$$

$$p = \frac{n_i^2}{N_D}$$

$$p \propto \frac{1}{N_D}$$

03. Ans: (b)

Sol: $V = 5\text{V}$

$$L = 100 \text{ mm}$$

$$\mu_n = 3800 \text{ cm}^2/\text{V-sec}$$

$$\mu_p = 1800 \text{ cm}^2/\text{V-sec}$$

$$V_{dn} = \mu_n E$$

$$= 3800 \times \frac{V}{L}$$

$$= 3800 \times \frac{5}{100 \times 10^{-1}}$$

$$= 1900 \text{ cm/sec}$$

04. Ans: (d)

Sol: For the n-type semiconductor with $n = N_D$ and $p = n_i^2 / N_D$, the hole concentration will fall below the intrinsic value because some of the holes recombine with electrons.

05. Ans: (c)

Sol: $N_A = \frac{10^{15}}{1.6} \text{ acceptor/cm}^3$

$$\mu_n = 4000 \text{ cm}^2/\text{V-sec}$$

$$\mu_p = 2000 \text{ cm}^2/\text{V-sec}$$

$$\sigma_p = p q \mu_p$$

$$= N_A q \mu_p \quad (\because 100\% \text{ doping efficiency})$$

$$= \frac{10^{15}}{1.6} \times 1.6 \times 10^{-19} \times 2000$$

$$= 0.2 \text{ mho/cm}$$

06. Ans: (d)

Sol: According to mass action law.

$$np = n_i^2$$

$$n_n p_n = n_i^2$$

$$n_p p_p = n_i^2$$

$$n_p N_A \approx n_i^2$$

$$N_D p_n \approx n_i^2$$

07. Ans: (a)

Sol: $R_H = 3.6 \times 10^{-4} \text{ m}^3/\text{c}$

$$\rho = 9 \times 10^{-3} \Omega\text{-m}$$

Let us consider n-type semiconductor

$$R_H = \frac{1}{nq}$$

$$n = \frac{1}{qR_H}$$

$$= \frac{1}{1.6 \times 10^{-19} \times 3.6 \times 10^{-4}}$$

$$= 1.736 \times 10^{22} \text{ m}^{-3}$$

08. Ans: (b)

Sol: At equilibrium

No. of e^- density = No. of hole density

$\therefore$ given e^- density is $n(x_1) = 10 n(x_2)$

$\Rightarrow n(x_1)$ is majority

$\Rightarrow n(x_2)$ is minority

$\therefore P(x_2) = 10P(x_1)$

09. Ans: (b)

Sol: $\rho_p = 3 \times 10^3 \Omega - \text{m}$

$\mu_p = 0.12 \text{ m}^2/\text{V-sec}$

$V_H = 60 \text{ mV}$

$$\rho_p = \frac{1}{\sigma_p}$$

$$3 \times 10^3 = \frac{1}{pq\mu_p}$$

$$p = \frac{1}{3 \times 10^3 \times 1.6 \times 10^{-19} \times 0.12}$$

$$P = 1.736 \times 10^{16} \text{ m}^{-3}$$

$$R_H = \frac{1}{pq}$$

$$= \frac{1}{1.736 \times 10^{16} \times 1.6 \times 10^{-19}}$$

$$= 360 \text{ m}^3/\text{C}$$

10. Ans: (b)

Sol: $J_{\text{drift}} = n\mu_n qE + p\mu_p qE$

$$J_{\text{drift}} = [(n.q)\mu_n + (p.q)\mu_p]E$$

$$J_{\text{drift}} = [\rho_n \mu_n + \rho_p \mu_p]$$

$$J \propto \rho$$



Charge concentration

11. Ans: (c)

Sol: $D_n = 20 \text{ cm}^2/\text{s}$

$\mu_n = 1600 \text{ cm}^2/\text{V-s}$

$$\frac{D}{\mu} = \frac{kT}{q} = V_T$$

$$\Rightarrow V_T = \frac{20}{1600} = 12.5 \text{ mV}$$

12. Ans: (d)

Sol: Conductivity of a semiconductor,

$$\sigma = (n\mu_n + p\mu_p)q$$

Where, $\mu_n \rightarrow$ mobility of electrons

$\mu_p \rightarrow$ mobility of holes

$n \rightarrow$ electron concentration

$p \rightarrow$ hole concentration

$q \rightarrow$ electron charge

13. Ans: (c)

Sol: $N_A = 2.29 \times 10^{16}$

$$E_{Fi} - E_{Fp} = kT \ln \left(\frac{N_A}{n_i} \right)$$

$$= 0.02586 \ln \left(\frac{2.29 \times 10^{16}}{1.5 \times 10^{10}} \right)$$

$$= 0.3682 \text{ eV}$$

$$\approx 0.37 \text{ eV}$$

14. Ans: (b)

Sol: Given,

2 wires $\therefore W_1$ & W_2

$d_2 = 2d_1$ where d = diameter of wire

$L_2 = 4L_1$ where L = length of wire

Relation between resistances of

W_1 & W_2

$$R = \frac{\rho \cdot L}{A} = \frac{\rho L}{\pi r^2} \quad r = \frac{d}{2}$$

$$R = \frac{\rho \cdot L}{\pi \frac{d^2}{4}} = \frac{4\rho L}{\pi d^2} \quad R \propto \frac{L}{d^2}$$

$$\frac{R_1}{R_2} = \frac{\frac{L_1}{d_1^2}}{\frac{L_2}{d_2^2}} = \frac{L_1}{d_1^2} \times \frac{d_2^2}{L_2} = \frac{L_1}{d_1^2} \times \frac{(2d_1)^2}{4L_1}$$

$$\Rightarrow \frac{R_1}{R_2} = 1 \quad \therefore R_1 = R_2$$

15. Ans: (c)

Sol: Hall voltage, V_H is inversely proportional to carrier concentration

$$\Rightarrow \frac{V_{H2}}{V_{H1}} = \frac{P_1}{P_2} = \frac{P_1}{2P_1}$$

$$\therefore V_{H2} = \frac{1}{2} V_{H1}$$

16. Ans: (b)

$$\text{Sol: } \frac{D}{\mu} = \frac{kT}{q} = V_T$$

$$\therefore D = \frac{0.36 \times 1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}}$$

$$= 9.315 \times 10^{-3} \text{ m}^2/\text{sec}$$

Diffusion length, $L = \sqrt{D\tau}$

$$= \sqrt{9.315 \times 10^{-3} \times 340 \times 10^{-6}}$$

$$= 1.77 \times 10^{-3} \text{ m}$$

17. Ans: (a)

Sol: In intrinsic semiconductor,

No. of e^- = No. of holes

18. Ans: (a)

Sol: In P-type, as doping increases hole concentration p increases. According

to mass action law $n_p = \frac{n_i^2}{p_p} \Rightarrow$ electron

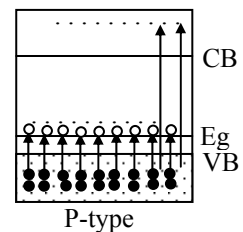
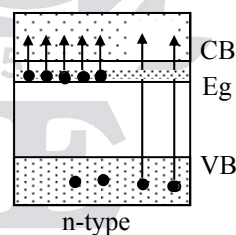
concentration decreases.

19. Ans: (b)

Sol: In intrinsic semiconductor, electron hole pairs are generated due to external energy $\Rightarrow$ true. electron mobility is 2 to 3 times more than hole mobility $\Rightarrow$ true. Both the statements are true but statement II is not a correct explanation of statement I.

20. Ans: (a)

Sol: Both statement (I) and (II) are true and statement (II) is the correct explanation of statement (I).



Conventional Practice Solutions
01.
Sol: $V = \mu E$

$$E = \frac{V}{\ell} = \frac{6V}{2\text{cm}} = 3V/\text{cm}$$

$$\mu = \frac{10^4}{3} = 3333.3 \text{ cm}^2/\text{V-sec}$$

02.
Sol: $J_{\text{drift}} = \sigma E = n\mu_e E = n\mu v$

$$\therefore v = \mu E$$

Given

$$E = 5\text{kV}/\text{cm} = 10^{16} \times 1.6 \times 10^{-19} \times 10^7 \text{ cm/sec}$$

$$N_d = 10^{16}/\text{cm}^3 = 1.6 \times 10^{-3} \times 10^7$$

$$v_s = 10^7 \text{ cm/sec}, J_{\text{drift}} = 1.6 \times 10^4 \text{ cm/sec}$$

Ohm's law valid for E is small

$$J_{\text{drift}} = 16000 \text{ A/cm}^2$$

03.

$$\text{Sol: } R_H = \frac{1}{\rho} = \frac{V_H W}{B I} = \frac{1 \times 10^{-3} \times 2 \times 10^{-3}}{0.1 \times 10 \times 10^{-3}}$$

$$= 2 \times 10^{-3}$$

$$R_H = \frac{1}{\rho} = \frac{1}{qn}$$

$$\Rightarrow n = \frac{1}{qR_H} = \frac{1}{1.6 \times 10^{-19} \times 2 \times 10^{-3}}$$

$$= 3.125 \times 10^{21} / \text{m}^3$$

04.
Sol: Note: Here all are in meters go with that

$$E_F - E_i = kT \ln \left(\frac{n}{n_i} \right) \quad n \approx N_D$$

$$(a) P_o = \frac{n_i^2}{n} = \frac{(1.6 \times 10^{16})^2}{10^{23}} = 2.5 \times 10^9 / \text{m}^3$$

$$(b) \sigma = nq\mu_n$$

$$= 2000 \Omega\text{-m}$$

$$(c) E_F - E_i = kT \ln \left(\frac{N_D}{n_i} \right) = 26\text{mV} \ln \left(\frac{10^{23}}{1.6 \times 10^{16}} \right)$$

$$E_F - E_i = 26 \times \ln \left(\frac{10^7}{1.6} \right) = 0.405 \text{ eV}$$

05.
Sol: $N_D = 10^{17}/\text{cm}^3, n_i = 1.5 \times 10^{10}/\text{cm}^3$

Hole concentration

$$p_n = \frac{n_i^2}{N_D} = \frac{2.25 \times 10^{20}}{10^{17}} = 2.25 \times 10^3 / \text{cm}^3$$

Fermi level of the sample with respect to intrinsic Fermi level

$$E_{F_n} - E_{F_i} = kT \ln \left(\frac{N_D}{n_i} \right)$$

$$= 0.026 \ln \left(\frac{10^{17}}{1.5 \times 10^{10}} \right)$$

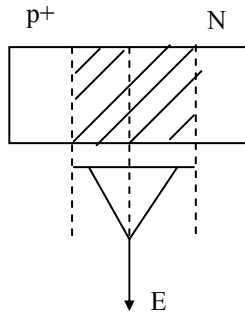
$$= 0.408 \text{ eV}$$

Chapter 2 PN Junction Diode

Objective Practice Solutions

01. Ans: (c)

Sol:



In P^+ , '+' indicates heavily region and 'n' indicates lightly doped region.

02. Ans: (a)

$$\text{Sol: } w = \sqrt{\frac{2\epsilon V_0}{q} \left[\frac{1}{N_D} + \frac{1}{N_A} \right]}$$

$$\frac{w_2}{w_1} = \sqrt{\frac{V_0 - V_{R2}}{V_0 - V_{R1}}}$$

$$\frac{w_2}{2\mu\text{m}} = \sqrt{\frac{0.8 - (-7.2)}{0.8 - (-1.2)}}$$

$$w_2 = 4 \mu\text{m}.$$

03. Ans: (a)

$$\text{Sol: } I = \left[\frac{AeD_p p_{n0}}{L_p} + \frac{AeD_n n_{p0}}{L_n} \right]$$

$$\Rightarrow I = \frac{AeD_p p_{n0}}{L_p}$$

$$\frac{I}{A} = \frac{eD_p p_{n0}}{L_p}$$

$$= \frac{1.602 \times 10^{-19} \times 12 \times 10^{12}}{1 \times 10^{-3}}$$

$$= 1.92 \text{ mA/cm}^2$$

04. Ans: (c)

$$\text{Sol: } 1 \text{ mA} = I_{GO}(e^{V_G/\eta V_T} - 1) = I_{SO}(e^{V_S/\eta V_T} - 1)$$

$$\frac{I_{GO}}{I_{SO}} = \frac{e^{0.718/(2 \times 0.026)}}{e^{0.1435/(1 \times 0.026)}} \cong 4000 = 4 \times 10^3$$

05. Ans: (c)

Sol: In a PN Junction diode the dynamic

$$\text{conductance } g_m = \frac{\Delta I}{\Delta V}, g_m = \frac{I_C}{V_T}$$

$$\text{i.e. } g_m \propto I_C$$

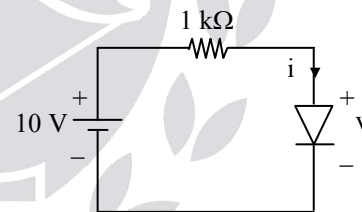
06. Ans: (d)

Sol: $i-v$ characteristic of the diode

$$i = \frac{v - 0.7}{500} \text{ A}, v \geq 0.7 \text{ V} \quad \dots (1)$$

From the given circuit, Loop equation :

$$v = 10 - 1000 i, v \geq 0.7 \text{ V} \quad \dots (2)$$



Eliminating 'v' from (1) and (2) :

$$i = \frac{10 - 1000 i - 0.7}{500} = \frac{9.3}{500} - 2i$$

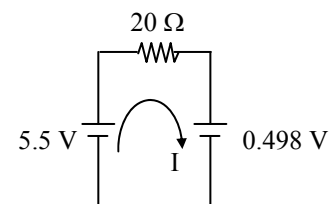
$$3i = \frac{9.3}{500}, i = \frac{3.1}{500} \text{ A} = 6.2 \text{ mA}$$

07. Ans: (b)

Sol: Given,

$$V_\gamma = 0.498 \text{ V}$$

$$V_T = 2 \text{ mV}$$



$$\therefore I = \frac{5.5 - 0.498}{20}$$

$$= 0.2501 \Rightarrow 250 \text{ mA}$$

08. Ans: (a)

Sol: Given $I_2^1 = I_1 \times 32$

Given $T_1 = 40^\circ\text{C}$ $T_2 = ?$

$$I_2^1 = I_1 \left(2^{\frac{T_2 - T_1}{10}} \right)$$

$$I_1 \times 32 = I_1 \left(2^{\frac{T_2 - T_1}{10}} \right)$$

$$2^5 = 2^{\frac{T_2 - T_1}{10}}$$

$$\Rightarrow \frac{T_2 - T_1}{10} = 5$$

$$T_2 - T_1 = 50$$

$$T_2 = 90^\circ\text{C}$$

$$T_2 = 50 + T_1$$

09. Ans: (b)

Sol: For either Si (or) Ge

$$\frac{dV}{dT} \cong -2.5 \text{ mV}/^\circ\text{C}$$

To maintain constant current

$$\frac{(V_2 - 700 \text{ mV})}{(40 - 20)} \frac{V}{^\circ\text{C}} = -2.5 \times 10^{-3} \frac{V}{^\circ\text{C}}$$

$$\rightarrow V_2 = 650 \text{ mV} \cong 660 \text{ mV}$$

10. Ans: (b)

$$\text{Sol: } C = \frac{\epsilon_0 \epsilon_r A}{d} \Rightarrow \frac{C}{A} = \frac{\epsilon_0 \epsilon_r}{d}$$

$$= \frac{11.7 \times 8.85 \times 10^{-12}}{10 \times 10^{-6}}$$

$$= 10 \mu\text{F}$$

11. Ans: (d)

Sol: The cut-in voltage for Germanium diode is 0.3 volt whereas the cut-in voltage for silicon diode is 0.7. So, cut-in voltage for silicon diode is greater than that for Germanium. Therefore, statement-I is false.

The reverse saturation current of Germanium diode is in the order of ' μA ' whereas that for silicon diode is ' nA '. So, Germanium diode has a higher reverse saturation current than silicon diode. Therefore, statement-II is true.

12. Ans: (b)

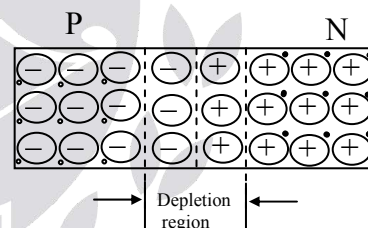
Sol: In all practical cases, the reverse saturation current (I_0) increased by 7% per $^\circ\text{C}$ rise in temperature. I_0 approximately doubles for every 10°C temperature rise for both Si and Ge materials. So, Statement-I is true.

In practical cases, $\frac{dV_0}{dT} = -2.5 \text{ mV}/^\circ\text{C}$ i.e., at

room temperature, the p-n junction voltage decreases by about 2.5 mV per $^\circ\text{C}$ with rise in temperature. So, statement-II is true but not the correct explanation of statement-I.

13. Ans: (c)

Sol:



The depletion region of an unbiased pn-junction contains negative ions in the p-side and positive ions in the n-side. So, an unbiased pn-junction develops a built-in potential at the junction with the n-side positive and the p-side negative. Therefore, statement-I is true.

The pn diode is a passive device. The pn-junction cannot behave as a battery. Therefore statement-II is false.

Conventional Practice Solutions

01.
Sol: $\sigma_n = N_D q \mu_n$

$$N_D = \frac{1}{1.6 \times 10^{-19} \times 1300} = \frac{10^{17}}{1.6 \times 13}$$

$$\sigma_p = N_A q \mu_p$$

$$N_A = \frac{100}{1.6 \times 10^{-19} \times 500} = \frac{10^{19}}{8}$$

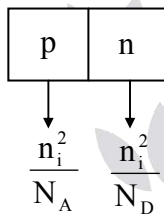
$$V_o = kT \ln \frac{N_D N_A}{n_i^2}$$

$$= 1.38 \times 10^{-23} \times 300 \ln \left(\frac{10^{17} \times 10^{19}}{1.6 \times 13 \times 8 \times 2.25 \times 10^{20}} \right)$$

$$= 0.799 \text{ V}$$

02.
Sol: From law of junction $P_1 = P_2 e^{V_{21}/V_T}$

$$V_{21} = V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$$



Shift in conduction band valency band

Height of the barrier

Linear/graded

$$V_o = kT \ln \left(\frac{N_A}{n_i} \right) + kT \ln \left(\frac{N_D}{n_i} \right)$$

$$V_o = kT \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

$$V_o = 0.25$$

03.

Sol: $V_o = kT \ln \frac{N_D N_A}{n_i^2} = 0.02586 \ln \left(\frac{10^{16} \times 10^{17}}{2.25 \times 10^{20}} \right)$

$$= 0.753$$

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{V_o} \right)^{1/2}}$$

 for non linear junction $\rightarrow \frac{1}{2}$

$$0.8 \text{ pF} = \frac{C_{j0}}{\left(1 + \frac{5}{0.753} \right)^{1/2}}$$

$$\Rightarrow C_{j0} = (0.8)(2.76)$$

$$= 2.211 \text{ pF}$$

04.

Sol: $I_D = I_s [e^{V_{be}/nV_T} - 1]$

 $n = 1$ for Ge

$$I_D = 2 \times 10^{-14} [e^{V_{be}/2V_T} - 1]$$

 $n = 2$ for Si

(a) $I_D = 50 \times 10^{-6}$

$$50 \times 10^{-10} = 2 \times 10^{-14} [e^{V_{be}/2V_T} - 1]$$

$$(25 \times 10^8 + 1) = e^{V_{be}/2V_T} \quad (\because V_T = 0.02586 \text{ V})$$

$$V_{be} = 1.1191 \text{ V}$$

(b) $I_D = 1 \text{ mA}$

$$10^{-3} = 2 \times 10^{-14} [e^{V_{be}/2V_T} - 1]$$

$$[5 \times 10^{10} + 1] = e^{V_{be}/2V_T}$$

$$V_{be} = 1.274 \text{ V}$$

05.

Sol: $V_{be1} = 0.2, V_{be2} = 0.6$

 Once D_1 becomes it acts like a voltage source so, D_2 never 'ON'

$$I_1 = \frac{100 - 0.2}{10k} = 9.98 \text{ mA}$$

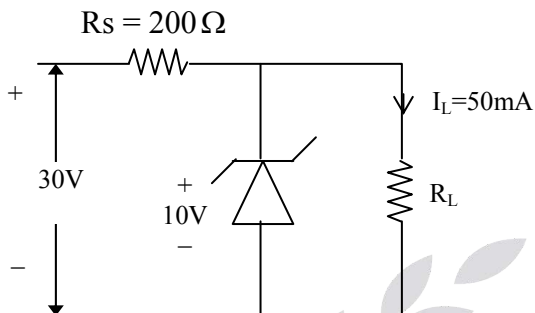
$$I_2 = 0 \text{ A}$$

Chapter 3 Zener Diode

Objective Practice Solutions

01. Ans: (d)

Sol:



$$V_s = 30 - 10 = 20V$$

$$\begin{aligned} \text{Power dissipation} &= \frac{V_s^2}{R_s} \\ &= \frac{20^2}{200} \\ &= 2 \text{ W} \end{aligned}$$

02. Ans: (c)

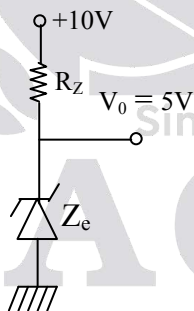
Sol: Power rating of Zener diode = 5 mW

$$I_z V_z = 5 \times 10^{-3}$$

$$I_z = \frac{5 \times 10^{-3}}{5} = 1 \text{ mA}$$

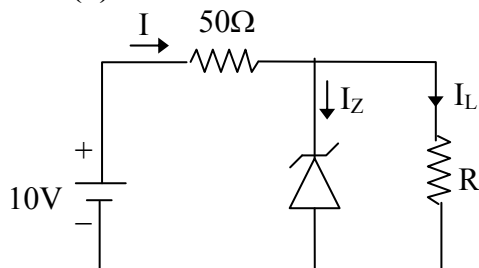
∴ Current flows through the circuit is = 1 mA

$$R_z = \frac{10 - 5}{1 \text{ m}} = 5 \text{ K}\Omega$$



03. Ans: (b)

Sol:



Given that, $V_z = 6V$

$$I_{z \min} = 5 \text{ mA}$$

$$R_{\min} \Rightarrow I_{L \max}$$

$$I = \frac{10 - 6}{50} = \frac{4}{50} = 80 \text{ mA}$$

$$I = I_{z \min} + I_{L \max}$$

$$I_{L \max} = 75 \text{ mA}$$

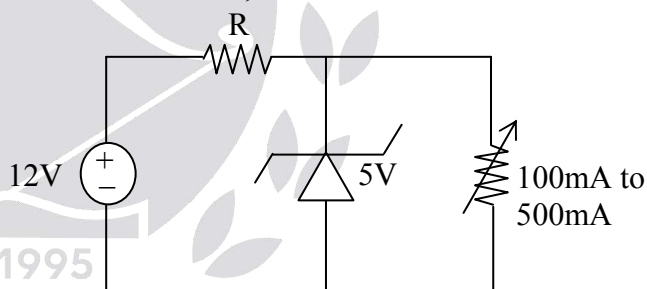
$$R_{L \min} = \frac{V_z}{I_{L \max}} = \frac{6}{75 \times 10^{-3}} = 80 \Omega$$

04. Ans: (b)

Sol: In -ve cycle of i/p diode forward biased, so replace by short circuit, so o/p = i/p with -12V in o/p only option 'b' exists, so using method of elimination answer is b.

05. Ans: (d)

Sol: Given circuit,



Given, source voltage

$$V_s = 12V$$

$$I_{L \min} = 100 \text{ mA}$$

$$I_{L \max} = 500 \text{ mA}$$

$$V_z = 5V$$

$$I_{z \min} = 0A$$

$$\therefore R = \frac{V_s - V_z}{I_{z \min} + I_{L \max}}$$

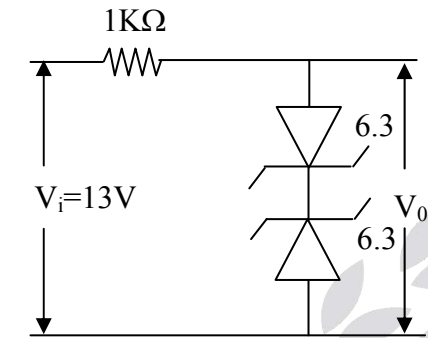
$$R = \frac{12 - 5}{500 \text{ mA}}$$

$$R = \frac{7 \times 10^3}{500}$$

$$R = \frac{70}{5} \Omega \quad R = 14 \Omega$$

06. Ans: (c)

Sol: Given circuit,



$$V_0 = 0.6 + 6.3 = 6.9 \text{ V}$$

07. Ans: (a)

Sol: The ideal characteristic of a stabilizer is constant output voltage with low internal resistance.

08. Ans: (a)

Sol:

- In PN junction diode break down depends on doping. As doping increases breakdown voltage decreases.
- In Zener diode breakdown is less than 6 V.
- It has Negative Temperature coefficient (operate in R. B).
- Avalanche diode breakdown greater than 6 V.

09. Ans: (b)

Sol: Both statement (I) and (II) are true but statement (II) is not a correct explanation of statement (I) because DC voltage stabilizer circuit can be implemented by using other components like Op-Amp also. There is no need that only Zener diode to be used.

Conventional Practice Solutions

01.

Sol: $V_i = 10\sin 100\pi t$

$$V_{be} = 0.7$$

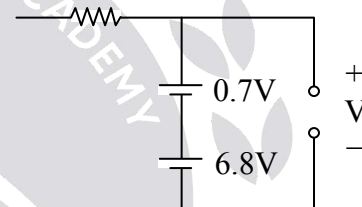
$$V_i < 0.7 \rightarrow D_1 - \text{OFF}, D_2 - \text{ON}$$

$$V = -0.7 = V_{\min}$$

$V_i > 0.7 \rightarrow D_1 - \text{ON}$, but zener diode in reverse bias.

If $V_i > 7.5 \rightarrow D_1 - \text{ON}$ and zener diode goes to breakdown.

$$\text{Then } V_0 = 7.5$$



02.

$$\text{Sol: } I = \frac{20 - 5.8}{1000\Omega}$$

$$I = 14.2\Omega$$

$$I_T = \frac{V_{\min}}{R_{\max}}$$

Case-I:

$$I = I_{\min} + I_{\max}$$

$$I_{\max} = 14.2 - 0.5 \\ = 13.7 \text{ mA}$$

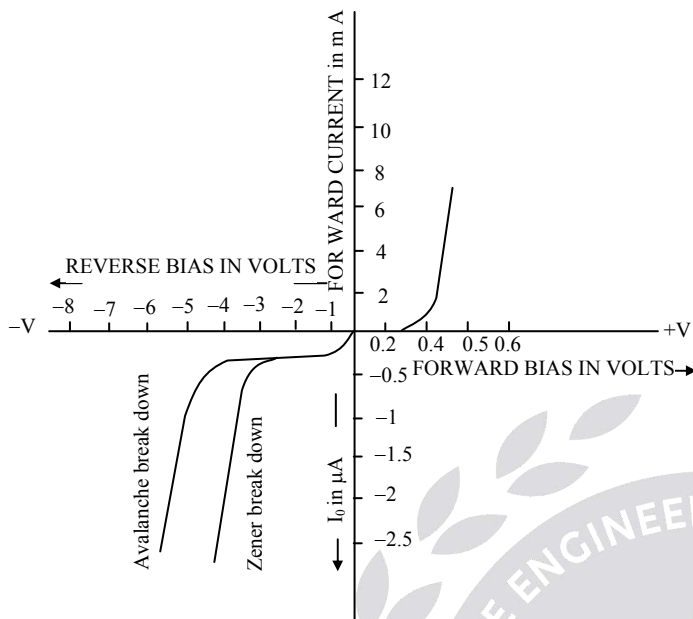
Case-II:

$$I_{\max} = 23.7 \text{ max (for } V_i = 30\text{V)}$$

In case -II if we give $V_i < 30\text{V}$, the zener diode goes to OFF state so, case-II fails.

03.

Sol:



When an ordinary **P-N junction diode** is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the **breakdown diode** many useful applications as a *voltage reference source*.

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs is called the *breakdown voltage*. The breakdown voltage depends on the width of

the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

Zener breakdown and Avalanche breakdown:

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction: (1) **Avalanche breakdown**

(2) **Zener breakdown.**

Avalanche breakdown:

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.

04

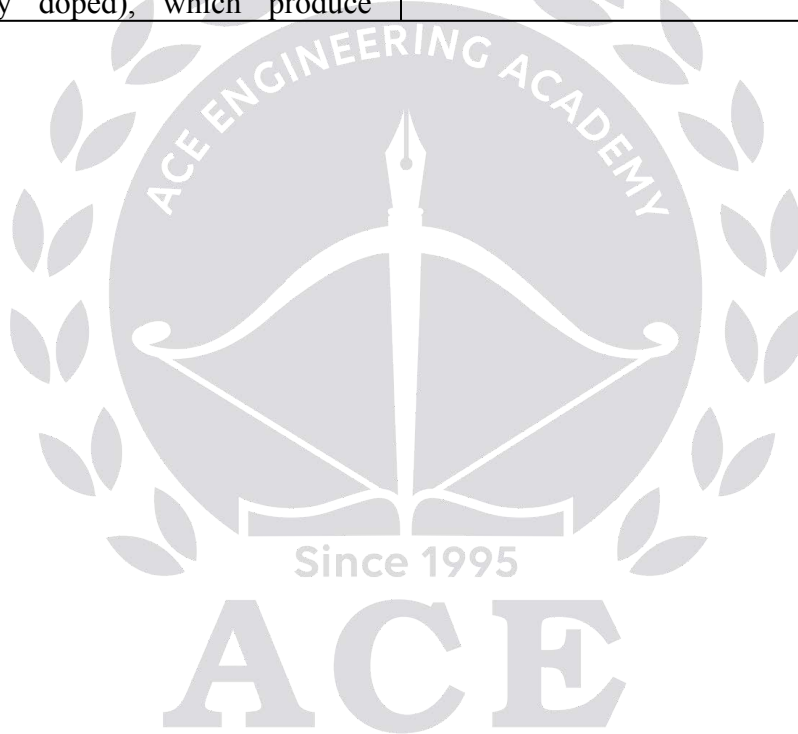
Sol: **Zener breakdown:**

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called

the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3×10^7 V/m.

Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5V are caused by Zener effect. Junctions that experience breakdown above 5V are caused by avalanche effect. Junctions that breakdown around 5V are usually caused by combination of two effects. The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce

narrow depletion layers. The avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers. With the increase in junction temperature Zener breakdown voltage is reduced while the avalanche breakdown voltage increases. The Zener diodes have a negative temperature coefficient while avalanche diodes have a positive temperature coefficient. Diodes that have breakdown voltages around 5V have zero temperature coefficient. The breakdown phenomenon is reversible and harmless so long as the safe operating temperature is maintained.



Chapter 4 Special Purpose Diodes

Objective Practice Solutions

01. Ans: (a)

Sol: Tunnel diode

It is highly doped S.C ($1 : 10^3$)

It is an abrupt junction (step) with both sides heavily doped made up of Ge (or) GaAs

It carries both majority and minority currents.

It can be used as oscillator

Operate in Negative Resistance region

Operate as fast switching device

02. Ans: (c)

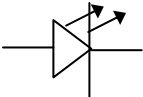
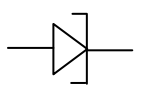
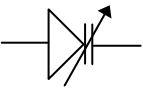
Sol: The values of voltage (V_D) across a tunnel-diode corresponding to peak and valley currents are V_P and V_V respectively. The range of tunnel-diode voltage V_D for which the slope of its I - V_D characteristics is negative would be $V_P \leq V_D < V_V$

03. Ans: (c)

Sol: Schottky diode is made of metal and semiconductor to decrease the switching times, hence it can be used for high frequency applications.

04. Ans: (a)

Sol:

Symbol	Circuit name	Applications
	LED	Direct Band gap
	Tunnel diode	Fast Switching circuits
	Varactor diode	Electronic Tuning

05. Ans: (a)

Sol: The tunnel diode has a region in its voltage current characteristics where the current decreases with increased forward voltage known as its negative resistance region. This characteristic makes the tunnel diode useful in oscillators and as a microwave amplifier.

Conventional Practice Solutions

01.

Sol: The **Schottky diode** (named after German physicist Walter H. Schottky, also known as **hot carrier diode**) is a semiconductor diode with a low forward voltage drop and a very fast switching action. When current flows through a diode there is a small voltage drop across the diode terminals. A normal silicon diode has a voltage drop between 0.6–1.7 volts, while a Schottky diode voltage drop is between approximately 0.15–0.45 volts.

This lower voltage drop can provide higher switching speed and better system efficiency.

Difference between Schottky Barrier Diode and P-N Junction Diode is as follows

Schottky Diode

- Usually using the aluminium metal which is trivalent element.
- Depletion layer is thinner than the p-n junction diode.
- Forward threshold voltage is smaller than p-n junction diode (0.1V).
- The junction capacitance is lower than p-n junction diode.

P-N Junction Diode

- Trivalent impurity is added to the pure silicon structure.
- Depletion layer is wider than Schottky diode.
- Forward threshold voltage is higher than Schottky diode (0.6V)
- The junction capacitance is higher than Schottky diode.

02.

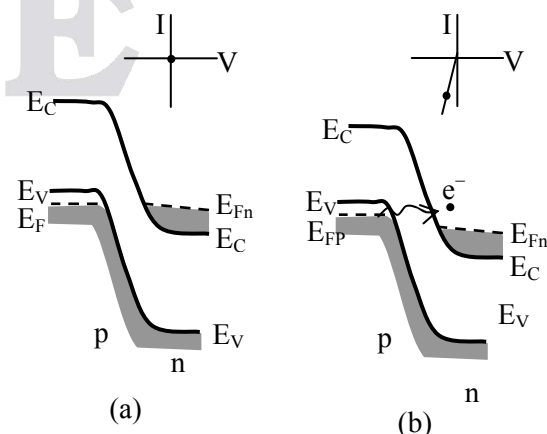
Sol:

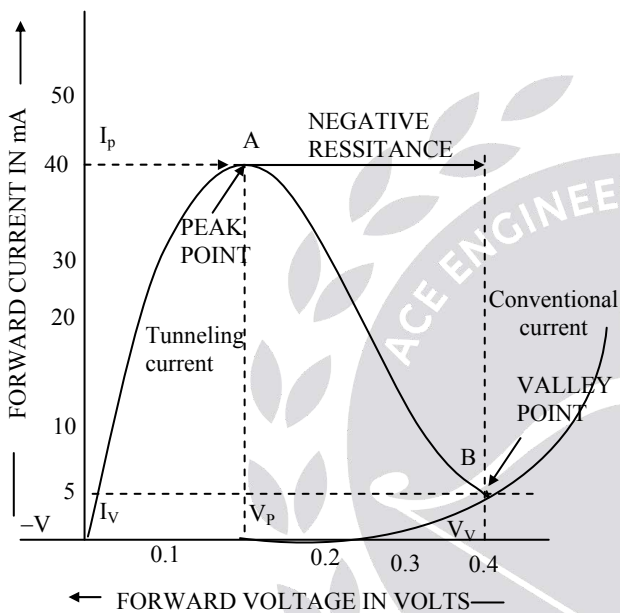
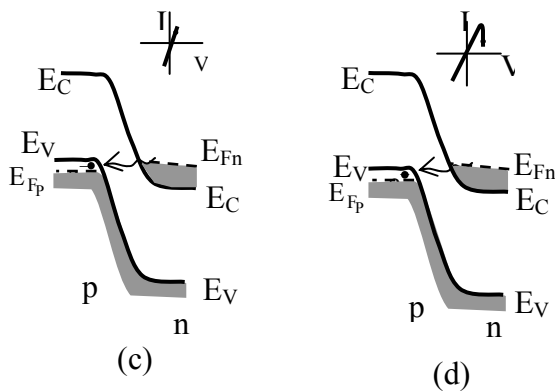
The solid state device shows negative incremental resistance is tunnel diode. The negative resistance region in tunnel diode is because of tunneling phenomena.

TUNNEL DIODE

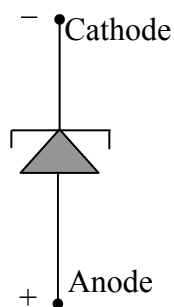
It is a high conductivity two terminal p-n junction doped heavily about 1000 times higher than a conventional junction diode. Such diodes are usually fabricated from germanium, gallium arsenide and gallium antimonide. Because of heavy doping, depletion layer width is reduced to an extremely small value of the order of 10^{-5} mm; reverse breakdown voltage is also reduced to a very small value (approaching zero) resulting in appearance of the diode to be broken for any reverse voltage, and a negative resistance section is produced in V-I characteristic of the diode.

Because of thin depletion layer, electrons are able to tunnel through the potential barrier at relatively low forward voltage (less than 50 mV). That is why such diodes are called tunnel diodes.





Tunneling Symbol:



V-I Characteristic of Tunnel Diode:

Figure 1: Tunnel diode band diagrams and I-V characteristics for various biasing conditions:

- (a) equilibrium (zero bias) condition, no net tunneling;
- (b) small reverse bias, electron tunneling from p to n;
- (c) small forward bias, electron tunneling from n to p;
- (d) increased forward bias, electron tunneling from n to p decreases as bands pass by each other

Forward bias produces immediate conduction. As soon as forward bias is applied, significant current is produced. The current quickly rises to the peak value, I_P when the applied forward voltage reaches a value V_P . The current variation in the vicinity of origin is due to quantum mechanical tunneling of electrons through narrow space charge region of the junction. With the further increase in forward voltage, the diode current starts reducing till it reaches to valley point B, the current decreases with the increase in voltage resulting in negative resistance in this region. In fact, this portion AB constitutes the most useful property of the diode. In this region the diode, instead of absorbing power, produces power. So the tunnel diode can be used as a very high frequency oscillator. For voltages higher than valley voltage V_V , current starts increasing as in any conventional diode. It can be used as an amplifier, an oscillator, or a switch. Because of very fast response to inputs, it is almost exclusively a high frequency component.

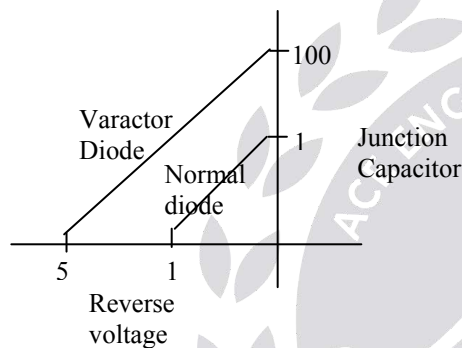
03.

Sol: A varactor diode is also known as varicap diode or epicap or voltcap diode or voltage variable capacitance or tuning diode. It behaves like variable capacitors. When reverse-biased, they have a capacitance that varies with an applied voltage. They are most often used in devices that require electronic tuning, such as radios.

Among the two capacitances, depletion capacitance (C_T) and diffusion capacitance (C_D), depletion capacitance is the effective capacitance used in varactor diode and varactor diode must be reverse biased to get the effective depletion layer.

$$C = \frac{\epsilon A}{w} \quad C \propto V_R^{-n}$$

The variation of junction capacitance with reverse voltage



$$C_T \propto \frac{1}{w}, \quad w = \frac{1}{\sqrt{\text{doping}}}$$

$$C_T \propto \sqrt{\text{doping}}$$

Generally, C_T will be 3pF for BJT and 5pF for diodes n is known as grading coefficient

$$n = \frac{1}{2} \text{ for step graded or abrupt junctions}$$

$$n = \frac{1}{3} \text{ for linear graded junctions}$$

$$n = \frac{1}{2.5} \text{ for diffused P-N junctions}$$

The popularly used material for varactor diode is GaAs.

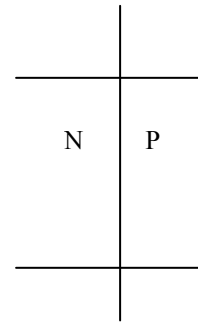


Fig. (a)

Abrupt doping profile

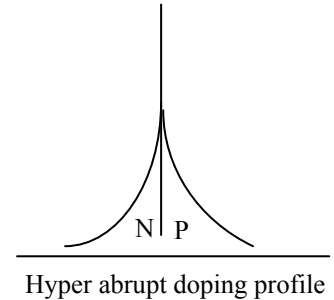
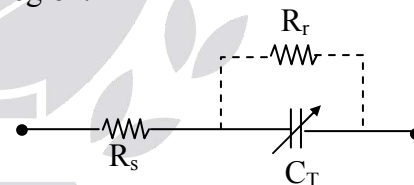


Fig. (b)

- The tuning range of varactor diode depends on doping levels.
- In the first case as shown in Fig(a). for uniform doping the tuning rate is 3:1 and 4:1
- To get the larger tunings some varactor diode will have hyper abrupt junctions as shown in Fig(b) and the tuning rate is 10:1.

Note:

Compared to ordinary diode varactor diode will have lightly doped N and lightly doped P region.



R_s – ohmic or contact resistance; $< 10\Omega$

R_r – reverse resistance ; $> 1M\Omega$

Applications:

Direct generation of FM by using varactor diode modulator circuit.

- Self balancing of AC bridges.
- LC resonating circuits.
- Fine tuning of receivers
- In parametric amplifiers, micro wave power amplifiers and satellite communications

04.

Sol: Schottky Contact:

A Schottky barrier refers to a metal-semiconductor contact having a large barrier height (i.e. $\phi_B > kT$) and low doping concentration that is less than the density of states in the conduction band or valence band.

The potential barrier between the metal and the semiconductor can be identified on an energy band diagram. To construct such a diagram we first consider the energy band diagram of the metal and the semiconductor, and align them using the same vacuum level.

As the metal and semiconductor are brought together, the Fermi energies of the two materials must be equal at thermal equilibrium.

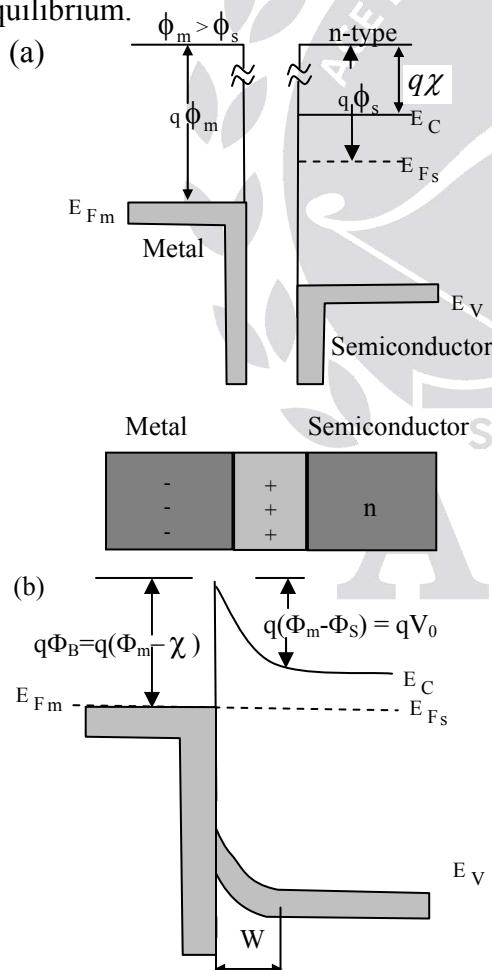


Figure: 1. A Schottky barrier formed by contacting an n-type semiconductor with a metal having a larger work function: (a) band diagram for the metal and the semiconductor before joining; (b) equilibrium band diagram for the junction.

The barrier height ϕ_B is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carrier resides.

For n-type semiconductors the barrier height is obtained

$$q\phi_B = q(\phi_m - \chi)$$

When a metal with work function $q\Phi_m$ is brought in contact with a semiconductor having a work function $q\Phi_s$, charge transfer occurs until the Fermi levels align at equilibrium (Fig:1). For example, when $\Phi_m > \Phi_s$, the semiconductor Fermi level is initially higher than that of the metal before contact is made. To align the two Fermi levels, the electrostatic potential of the semiconductor must be raised (i.e., the electron energies must be lowered) relative to that of the metal. In the n-type semiconductor of Fig: 1(a) depletion region W is formed near the junction. The positive charge due to uncompensated donor ions within W matches the negative charge on the metal. The electric field and the bending of the bands within W are similar to p-n junctions.

The equilibrium contact potential V_0 , which prevents further net electron diffusion from the semiconductor conduction band into the metal, is the difference in work function potentials $\Phi_m - \Phi_s$. The potential barrier height Φ_B for electron injection from the metal into the semiconductor conduction band is $\Phi_m - \chi$, where χ (called the electron affinity) is measured from the

vacuum level to the semiconductor conduction band edge. The equilibrium potential difference V_0 can be decreased or increased by the application of either forward or reverse bias voltage, as in the p-n junction.

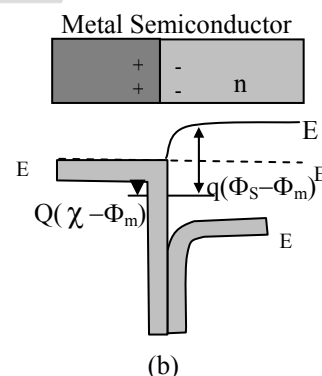
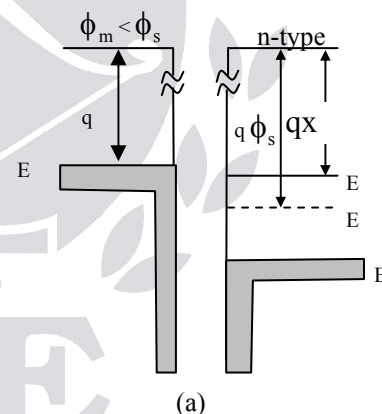
Ohmic Contacts:

An ohmic contact is defined as a metal-semiconductor contact that has a negligible contact resistance relative to the bulk or series resistance of the semiconductor. A satisfactory ohmic contact should not significantly degrade device performance and can pass the required current with a voltage drop that is small compared with the drop across the active region of the device. An ohmic metal semiconductor contact having a linear I-V characteristic in both biasing directions. For example, the surface of a typical integrated circuit is a maze of p and n regions, which must be contacted and interconnected. It is important that such contacts be ohmic, with minimal resistance and no tendency to rectify signals.

Ideal metal-semiconductor contacts are ohmic when the charge induced in the semiconductor in aligning the Fermi levels is provided by majority carriers (Fig.2). For example, in the $\Phi_m < \Phi_s$ (n-type) case of Fig.2(a), the Fermi levels are aligned at equilibrium by transferring electrons from the metal to the semiconductor. This raises the semiconductor electron energies (lowers the electrostatic potential) relative to the metal at equilibrium (Fig. 2(b)). In this case the barrier to electron flow between the metal and the semiconductor is small and easily overcome by a small voltage. Similarly, the case $\Phi_m > \phi_s$ (p-type) results in easy hole flow across the junction (Fig: 2(d)). There is no depletion region occurs in

the semiconductor in these cases since the electrostatic potential difference required to align the Fermi levels at equilibrium calls for accumulation of majority carriers in the semiconductor.

A practical method for forming ohmic contacts is by doping the semiconductor heavily in the contact region. Thus if a barrier exists at the interface, the depletion width is small enough to allow carriers to tunnel through the barrier. For example, Au containing a small percentage of Sb can be alloyed to n-type Si, forming an n^+ layer at the semiconductor surface and an excellent ohmic contact. Similarly, p-type material requires a p^+ surface layer in contact with the metal. In the case of Al on p-type Si, the metal contact also provides the acceptor dopant. Thus the required p^+ surface layer is formed during a brief heat treatment of the contact after the Al is deposited.



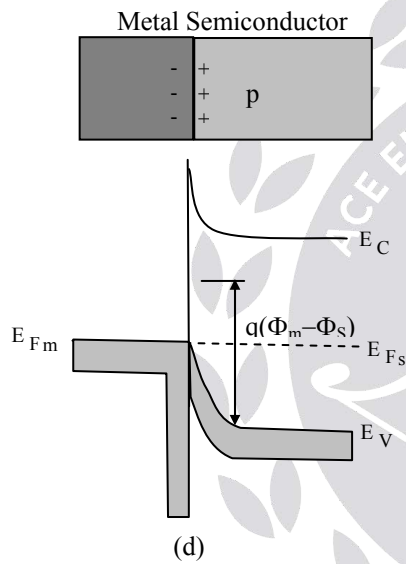
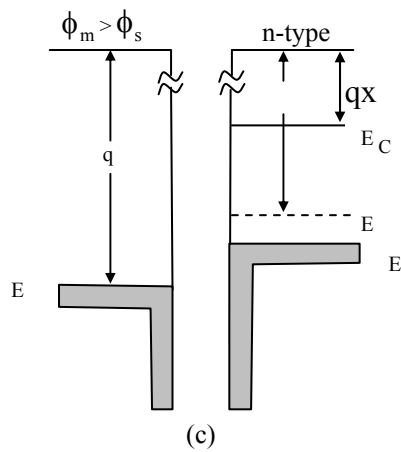


Figure.2: Ohmic metal-semiconductor contacts: (a) $\phi_m < \phi_s$ for an n-type semiconductor, and (b) the equilibrium band diagram for the junction; (c) $\phi_m > \phi_s$ for a p-type semiconductor, and (d) the junction at equilibrium.

Chapter 5 Bipolar Junction Transistor

Objective Practice Solutions

01. Ans: (b)

Sol: $\alpha = \beta/(1+\beta) = 0.9803$

$$\alpha = \beta^* \gamma^*$$

$$\rightarrow \beta^* = 0.9803/0.995 \\ = 0.9852$$

02. Ans: (d)

Sol: $I_C = 4\text{mA}$

$$r_0 > 20\text{k}\Omega$$

$$r_0 = \frac{V_A}{I_C}$$

$$\frac{V_A}{I_C} > 20\text{k}\Omega$$

$$V_A > 20\text{k}\Omega \times I_C$$

$$V_A > 20 \times 10^3 \times 4 \times 10^{-3}$$

$$V_A > 80$$

03. Ans: (b)

Sol: $V_A = 100\text{V}$

$$I_C = 1\text{mA}$$

$$V_{CE} = 10\text{V}$$

$$I_{CQ} \left(1 + \frac{V_{CE}}{V_A} \right) = I_C$$

$$\text{If } V_A \rightarrow \infty$$

$$\Rightarrow I_C = I_{CQ} = 1\text{mA}$$

04. Ans: (b)

Sol: The phenomenon is known as “Early Effect” in a bipolar transistor refers to a reduction of the effective base-width caused by the reverse biasing of the base-collector junction.

05. Ans: (a)

Sol: Given $\alpha = 0.995$, $I_E = 10\text{mA}$,

$$I_{C0} = 0.5\text{mA}$$

$$I_{CEO} = (1 + \beta) I_{CBO}$$

$$I_{CEO} = \left(1 + \frac{\alpha}{1 - \alpha} \right) I_{CBO}$$

$$I_{CEO} = (1 + 199) \times 0.5 \times 10^{-6}$$

$$I_{CEO} = 100\mu\text{A}$$

06. Ans: (a)

Sol: I_{CBO} is equal to I_{CO} . Reverse leakage current double for every 10°C rise in temperature.

07. Ans: (b)

Sol: Given base width $W_B = 50 \times 10^{-6}\text{cm}$

$$\text{Base doping } N_B = 2 \times 10^{16}\text{cm}^{-3}$$

$$\epsilon_r \epsilon_0 = \epsilon \quad \epsilon = 10^{-12}\text{F/cm}$$

$$V_{\text{punch}} = \frac{q N_B W_B^2}{2 \epsilon}$$

$$= \frac{1.6 \times 10^{-19} \times 2 \times 10^{16} \times (50 \times 10^{-6})^2}{2 \times 10^{-12}}$$

$$V_{\text{punch}} = \frac{1.6 \times 2 \times 2500}{2} \times 10^{-3} = 4\text{V}$$

08. Ans: (a)

Sol: $\alpha = 0.98$

$$I_B = 40\mu\text{A}$$

$$I_{CBO} = 1\mu\text{A}$$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$$

For a CE active BJT

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

$$= 49 \times 40 \times 10^{-6} + 50 \times 10^{-6}$$

$$= 2.01\text{mA}$$

09. Ans: (b)

Sol: $I_{CBO} = 0.4 \mu A$

$$I_{CEO} = 60 \mu A$$

$$I_{CEO} = (1 + \beta) I_{CBO}$$

$$1 + \beta = \frac{I_{CEO}}{I_{CBO}}$$

$$= \frac{60}{0.4}$$

$$= 150$$

$$\beta = 150 - 1$$

$$= 149$$

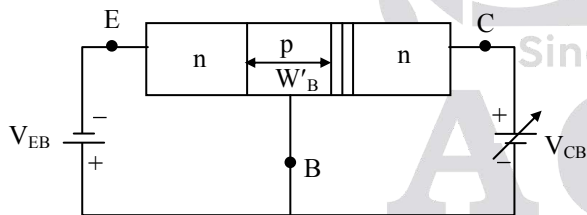
$$\alpha = \frac{\beta}{1 + \beta}$$

$$= \frac{149}{150}$$

$$= 0.993$$

10. Ans: (c)

Sol: Variation of base width due to reverse biased voltage across collector - base junction is known as "Early Effect".



As V_{CB} increases, effective base width (W'_B) decreases.

11. Ans: (a)

Sol: Both statement (I) and (II) are true and statement (II) is the correct explanation of statement (I).

At very high temperature, extrinsic semiconductors will behave as intrinsic i.e., charge carriers will remain constant.

12. Ans: (b)

Sol:

Junction		Region of operation
E - B	C - B	
F. B	F.B	Saturation Region
F.B	R.B	Active Region
R.B	F.B	Inverse active Region
R.B	R.B	Cut-off Region

13. Ans: (c)

Sol: High power transistors are made of Si to withstand high temperature: Silicon is an indirect band gap material.

Conventional Practice Solutions

01.

Sol: $I_C = \beta I_B$

$$\beta = \frac{I_C}{I_B} = \frac{2.7 \times 10^{-3}}{50 \times 10^{-6}} = 54$$

$$\alpha = \frac{\beta}{1 + \beta} = \frac{54}{55} = 0.981$$

02.

Sol: $I_E = I_{pE} + I_{nE} = 1.3 \text{ mA}$

Given npn transistor

$$r^* = \frac{I_{nE}}{I_E} = \frac{1.2 \times 10^{-3}}{1.3 \times 10^{-3}} = 0.923$$

Emitter efficiency

$$(\beta^*) = \frac{I_{nC}}{I_{nE}} = \frac{1.18}{1.2} = 0.983$$

Base transport factor

$$\alpha = \frac{I_{nC}}{I_E} = \beta^* r^* = 0.907$$

03.

Sol: $I_E = I_B + I_C$

$$\begin{aligned} I_3 &= I_1 + I_2 \\ &= 275 \mu\text{A} + 125 \mu\text{A} \\ &= 400 \mu\text{A} \end{aligned}$$

04.

Sol:

$$(a) -5 + (10k)I_B + V_{BE} = 0$$

$$I_B = \frac{5 - 0.7}{10k} = 0.43 \text{ mA}$$

$$(b) I_C = \beta I_B = 43 \text{ mA}$$

$$(c) I_E = I_B + I_C = 43.43 \text{ mA}$$

$$(d) -10 + (100)I_C + V_{CE} = 0$$

$$V_{CE} = 10 - (100)(43)(10^{-3}) = 5.7 \text{ V}$$

$$(e) V_{BE} - V_{CE} + V_{CB} = 0$$

$$V_{CB} = V_{CE} - V_{BE} = 5.7 - 0.7 = 5 \text{ V}$$

05.

Sol: Let us assume in active region

$$I_B = \frac{3 - 0.7}{10k} = 0.23 \text{ mA}$$

n	p	n
---	---	---

Here $V_B > V_E$

So, emitter junction is forward biased so, either it is in active or saturation region

$$-10 + I_C(1k) + V_C = 0$$

$$\begin{aligned} V_C &= 10 - [50 \times 0.23 \times 10^{-3}] 10^3 \\ &= -1.5 \text{ V} \end{aligned}$$

Here $V_E = 0$, $V_C = -1.5 \text{ V} \rightarrow$ it is not possible so, It is not in active region.

Hence it is in saturation region

$\rightarrow$ Now consider saturation region with

$$V_{CE} = 0.2 \text{ V}$$

$$I_B = 0.23 \text{ mA}$$

$$-10 + 1k(I_{C_{\text{sat}}}) + V_{CE_{\text{sat}}} = 0$$

$$I_{C_{\text{sat}}} = \frac{9.8}{1k} = 9.8 \text{ mA}$$

$$\beta_{\text{sat}} = \frac{I_{C_{\text{sat}}}}{I_B} = \frac{9.8}{0.23} = 42.608$$

$\beta_{\text{sat}} < \beta$ (which satisfies condition of saturation region)

Chapter 6 Junction Field Effect Transistor

Objective Practice Solutions

01. Ans: (d)

Sol: $V_G \rightarrow 4.2 \text{ V to } 4.4 \text{ V}$

$I_D \rightarrow 2.2 \text{ mA to } 2.6 \text{ mA}$

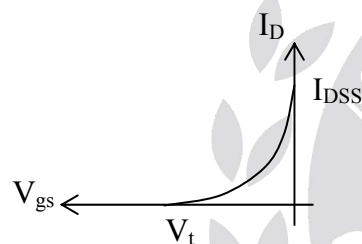
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$= \frac{(2.6 - 2.2) \times 10^{-3}}{4.4 - 4.2}$$

$$= 2 \text{ m}\Omega$$

02. Ans: (c)

Sol:



$$V_{GS} = V_t \quad I_D = 0$$

$$V_{GS} = 0 \quad I_D = I_{DSS}$$

03. Ans: (b)

Sol: $I_{Dmax} = I_{DSS} = 10 \text{ mA}$

$$V_P = -4 \text{ V}$$

$$V_{GS} = -1 \text{ V}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

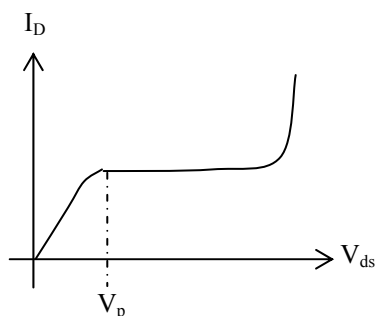
$$= 10 \times 10^{-3} \left(1 - \frac{-1}{-4} \right)^2$$

$$= 10 \times 10^{-3} \times \left(\frac{3}{4} \right)^2$$

$$= 5.625 \text{ mA}$$

04. Ans: (d)

Sol:



Drain current remains constant at pinch off region even if the drain voltage increases.

05. Ans: (c)

Sol: JFET acts as a voltage controlled current source.

06. Ans: (a)

Sol: Mobility of electron is higher than mobility of hole

Si

Electron mobility : $1350 \text{ cm}^2 / \text{v-s}$

Hole mobility : $450 \text{ cm}^2 / \text{v-s}$

Ge

Electron mobility : $3600 \text{ cm}^2 / \text{v-s}$

Hole mobility : $1800 \text{ cm}^2 / \text{v-s}$

: Low leakage current means high input impedance.

: Reverse bias increases, channel width reduces (wedge shaped).

07. Ans: (c)

Sol: $V_P = -8 \text{ V}$

$$I_{DSS} = 12 \text{ mA}$$

From the given circuit,

$$V_G = -5 \text{ V}$$

$$V_S = 0 \text{ V}$$

$$V_{GS} = -5 \text{ V}$$

V_{DS} at which pinch-off region means

$$\begin{aligned}(V_{DS})_{\min} &= V_{GS} - V_P \\ &= -5 - (-8) \\ &= -5 + 8 \\ &= 3 \text{ V}\end{aligned}$$

08. Ans: (d)

Sol: P. Voltage controlled device –FET (3)

Q. Current controlled device –BJT (1)

R. Conductivity modulation device--
IMPATT diode (4)

S. Negative conductance device -UJT (2)

09. Ans: (d)

Sol: $I_{DSS} = 12 \text{ mA}$

$$V_P = -6 \text{ V}$$

$$V_{GS} = 0 \text{ V}$$

$$V_{DS} = 7 \text{ V}$$

$$\text{At } V_{GS} = 0 \text{ V, } I_D = I_{DSS}$$

$$= 12 \text{ mA} \left(\because I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \right)$$

10. Ans: (d)

Sol:

Device :	Application
A. Diode	Rectifier (3)
B. Transistor	Amplifier (1)
C. Tunnel diode	Oscillator (2)
D. Zener diode	Reference Voltage (4)

11. Ans: (a)

$$\text{Sol: } g_{m0} = \left| \frac{2I_{DSS}}{V_P} \right| = \frac{2 \times 25 \times 10^{-3}}{10} = 5$$

12. Ans: (b)

Sol: BJT is current controlled current source

$$(R_i = 0 ; R_o = \infty)$$

Gain $\times$ B.W is high

FET is voltage controlled current source

$$(R_i = \infty ; R_o = 0)$$

Gain $\times$ B.W is low

UJT is a negative resistance device and can be used as an oscillator

UJT can be used as switch but can't be amplification.

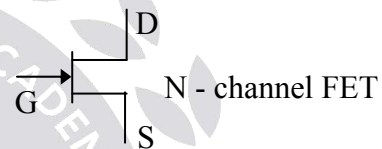
13. Ans: (a)

Sol: In FET majority carriers only exist.

In BJT majority & minority carriers exist.

14. Ans: (a)

Sol:



Input resistance of FET is of the order of tens (or) hundreds of mega ohms ($M\Omega$ s)

: V_{gs} is reverse bias.

: In reverse bias very small leakage current I_{CO} flows through the gate.

15. Ans: (c)

Sol: FET's has high input impedance when compared to BJT. Because of this FET's are more suitable at the input stage of millivoltmeter and CRO's than BJT's. Generally FET has input impedance in the range of several $M\Omega$.

Statement (II) is false. So, option 'c' is correct.

16. Ans: (d)

Sol: Statement (I) is false, because FET is a voltage control current source.

Statement (II) is true. Why because operation of FET does not depend on minority carrier i.e. FET operation depends on either electrons or holes as a majority carriers.

Conventional Practice Solutions

01.

Sol: Given data

$$a = 3 \times 10^{-4} \text{ cm}$$

$$N_D = 10^{15} \text{ cm}^{-3}$$

(i) Pinch-off voltage for n-channel JFET

$$V_P = \frac{-qN_D}{2\epsilon} a^2$$

$$\Rightarrow V_P = \frac{-1.6 \times 10^{-19} \times 10^{15}}{2 \times 11.7 \times 8.854 \times 10^{-14}} \times (3 \times 10^{-4})^2$$

$$V_P = -6.95 \text{ Volts}$$

(ii) The effective half channel height 'b' can be express as

$$b = a \left[1 - \sqrt{\frac{V_{GS}}{V_P}} \right]$$

$$b = 3 \times 10^{-4} \left[1 - \sqrt{\frac{\frac{1}{2} V_P}{V_P}} \right]$$

$$(\because \text{Given } V_{GS} = \frac{V_P}{2})$$

$$\Rightarrow b = 3 \times 10^{-4} \left[1 - \sqrt{\frac{1}{2}} \right]$$

$$\Rightarrow b = 0.87 \times 10^{-4} \text{ cm}$$

02.

Sol: Given data (for n-channel JFET)

Pinch-off voltage, $V_P = -3 \text{ V}$

$$I_{DSS} = 20 \text{ mA}$$

$$I_{GSS} = 5 \text{ nA at } 25^\circ \text{C}$$

As we know, the condition for zero temperature co-efficient

$$|V_{GS}| = |V_P| - 0.63$$

$$\Rightarrow |V_{GS}| = 3 - 0.63$$

$$\Rightarrow |V_{GS}| = 2.37 \text{ Volts}$$

$$\Rightarrow V_{GS} = -2.37 \text{ Volts}$$

$\therefore V_{GS} = -2.37 \text{ Volts}$ will give the JFET a zero temperature coefficient.

The resulting drain current ' I_D ' for $V_{GS} = -2.37 \text{ volts}$ is

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$\Rightarrow I_D = 20 \times 10^{-3} \left(1 - \frac{2.37}{3} \right)^2$$

$$\Rightarrow I_D = 0.882 \text{ mA}$$

$$I_{GSS} (\text{at } 50^\circ \text{C}) = I_{GSS} (25^\circ \text{C}) 2^{\frac{50-25}{10}}$$

$$\Rightarrow I_{GSS} (\text{at } 50^\circ \text{C}) = 5 \times 10^{-9} \times 2^{2.5}$$

$$\Rightarrow I_{GSS} (\text{at } 50^\circ \text{C}) = 28.28 \text{ nA}$$

03.

Sol: Given data

$$I_{DSS} = 20 \text{ mA}$$

$$V_{GS}(\text{off}) = V_P = -10 \text{ V}$$

$$\text{When } V_{GS} = 0, I_S = I_{DSS}$$

$$\Rightarrow \text{For } V_{GS} = 0, I_S = 20 \text{ mA}$$

The condition for saturation in JFET is

$$V_{DS} \geq V_{GS} - V_P$$

$$\Rightarrow V_{DS} \geq -2 + 10$$

$$\Rightarrow V_{DS} \geq 8 \text{ volts}$$

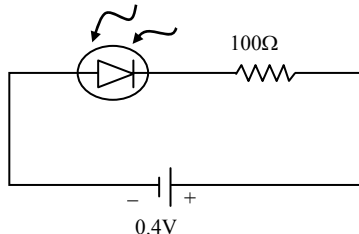
$\therefore$ For saturation $V_{DS} \geq 8 \text{ volts}$

Chapter 7 Optoelectronic Devices

Objective Practice Solutions

01. Ans: (a)

Sol:



By KVL,

$$0.4 - 100 \times 1.8 \times 10^{-3} - V_p = 0$$

$$V_p = 0.4 - 100 \times 1.8 \times 10^{-3}$$

$$= 0.22 \text{ V}$$

$$V_p = r_p I$$

$$r_p = \frac{V_p}{I}$$

$$= \frac{0.22}{1.8 \times 10^{-3}}$$

$$= 122.22 \Omega$$

02. Ans: (b)

Sol: If illumination doubled then current passing through the photo diode is doubled

$$I_D = 2 \times 1.8 = 3.6 \text{ mA}$$

Voltage across photo diode is

$$= 0.4 - 3.6 \times 10^{-3} \times 100$$

$$= 0.4 - 0.36$$

$$V_p = r_p I_p$$

$$r_p = \frac{V_p}{I_p}$$

$$= \frac{0.04}{3.6} \times 10^3$$

$$= 0.01111 \times 10^3$$

$$= 11.11 \Omega$$

03. Ans: (b)

Sol: Avalanche photo diodes are preferred over PIN diodes in optical communication because Avalanche photo diodes are (APDs), extracted from avalanche gain and excess noise measurement and higher sensitivity. PIN diodes generate more noise.

04. Ans: (c)

Sol: Photo diode always operates in reverse bias. When no light falls on photo diode, Small amount of reverse saturation current flows through the device called "dark current".

05. Ans: (a)

Sol: Give,

$$E_g = 1.12 \text{ eV}; \lambda_1 = 1.1 \mu\text{m}$$

$$\lambda_2 = 0.87 \mu\text{m}; E_{g2} = ?$$

$$E_g = \frac{12400 \text{ A}^0}{\lambda} \Rightarrow E_g \propto \frac{1}{\lambda}$$

$$\frac{E_{g1}}{E_{g2}} = \frac{\lambda_2}{\lambda_1}$$

$$\Rightarrow E_{g2} = E_{g1} \times \frac{\lambda_1}{\lambda_2} = 1.12 \times \frac{1.1}{0.87} = 1.416 \text{ eV}$$

06. Ans: (a)

Sol: Sensitivity of photo diode depends on light intensity and depletion region width.

07. Ans: (d)

$$\text{Sol: } I_D = \frac{24 - 1.8}{820} = 0.02707 \text{ A} = 27.07 \text{ mA}$$

08. Ans: (c)

Sol: Photo diode operate in R.B: Photo diode works on the principle of photo electric effect.

09. Ans: (b)

Sol: Voltage across PN junction diode resulting in current which in turn produce photons and light output. This inversion mechanism also called injection electro luminescence observed in LED's.

10. Ans: (b)

Sol: $\lambda = 890 \text{ A}^\circ$

$$\lambda = \frac{1.24 \times 10^{-6}}{E_G} \text{ m}$$

$$= \frac{1.24 \times 10^{-6}}{890 \times 10^{-10}}$$

$$= 13.93 \text{ eV}$$

11. Ans: (d)

Sol: Solar cell converts optical (sunlight) energy into electrical energy.

12. Ans: (b)

Sol: $R = 0.45 \text{ A/W}$

$$P_0 = 50 \text{ } \mu\text{W}$$

$$R = \frac{I_p}{P_0}$$

$$I_p = R P_0$$

$$= 0.45 \times 50$$

$$= 22.5 \text{ } \mu\text{A}$$

$$\text{Load current} = I_p + I_0$$

$$= 22.5 \text{ } \mu\text{A} + 1 \text{ } \mu\text{A}$$

$$= 23.5 \text{ } \mu\text{A}$$

13. Ans: (d)

Sol: LED: F.B

Photo diode: R.B

Zener diode: R.B

Ordinary diode: F.B

Tunnel diode: F.B

Variable capacitance diode: R.B

Avalanche diode: R.B

14. Ans: (c)

Sol: Tunnel diode is always operated in forward bias and light operated devices are operated in reverse bias. (Avalanche photo diode).

15. Ans: (b)

Sol: LED's and LASER's are used in forward bias.

Photo diodes are used in reverse bias.

16. Ans: (b)

Sol: Both statement (I) and (II) are true but statement (II) is not a correct explanation of statement (I).

17. Ans: (a)

Sol: Both statement (I) and (II) are true and statement (II) is the correct explanation of statement (I).

Conventional Practice Solutions

01.

Sol: Given, Forbidden energy gap $E_0 = 0.71\text{eV}$

Electron charge $e = 1.6 \times 10^{-19}\text{C}$

Plank's constant $h = 6.625 \times 10^{-34}\text{ joule - sec}$

Velocity of light $C = 3 \times 10^8\text{ m/sec}$

We know that, $E_0 = hf$

$$E_0 = h \frac{C}{\lambda} \Rightarrow \lambda = \frac{hC}{E_0}$$

$$\lambda = \frac{6.625 \times 10^{-34} \times 3 \times 10^8}{0.71 \times 1.6 \times 10^{-19}} = 1.74\mu\text{m}$$

OR

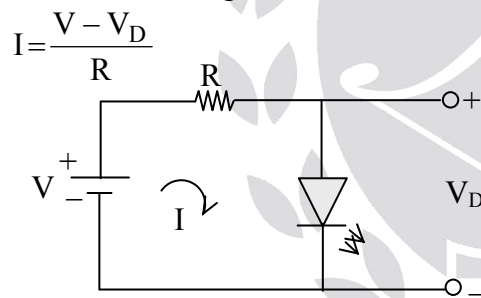
$$\lambda = \frac{12400}{E_2 - E_1} = \frac{12400}{E_c - E_v} = \frac{12400}{E_g} \text{A}^\circ$$

$$\lambda = \frac{12400}{0.71} \quad \lambda = 17465 \text{A}^\circ \text{ or}$$

$$\lambda = 1.7465\mu\text{m}$$

02.

Sol: The circuit arrangement is as shown below:



Given data, $V_{D\min} = 1.8\text{ V}$,
 $V_{D\max} = 3\text{ V}$

Case 1: Given data,

$V = 24\text{ V}$ & $R = 820\Omega$

Let the current through the LED is I_1 when

$V_D = V_{D\min}$ and current is I_2 when

$V_D = V_{D\max}$

$$I_1 = \frac{V - V_{D\min}}{R} = \frac{24 - 1.8}{820} = 27.07\text{ mA}$$

$$\therefore I_1 = 27.07\text{ mA}$$

$$\text{and } I_2 = \frac{V - V_{D\max}}{R} = \frac{24 - 3}{820} = 25.61\text{ mA}$$

$$\therefore I_2 = 25.61\text{ mA}$$

The change in the current flowing through the LED under minimum and maximum voltage drops across the diode is given by

$$dI = |I_1 - I_2|$$

$$dI = 1.46\text{ mA} \quad \dots\dots\dots (I)$$

Case 2:

Given data,

$V = 10\text{ V}$ & $R = 120\Omega$

$$\therefore I_1 = \frac{V - V_{D\min}}{R} = \frac{10 - 1.8}{120} = 68.33\text{ mA}$$

$$\therefore I_1 = 68.33\text{ mA}$$

$$\text{and } I_2 = \frac{V - V_{D\max}}{R} = \frac{10 - 3}{120} = 58.33\text{ mA}$$

$$\therefore I_2 = 58.33\text{ mA}$$

$$\therefore dI = |I_1 - I_2|$$

$$\therefore dI = 10\text{ mA} \quad \dots\dots\dots (II)$$

Conclusion: For an LED the brightness is directly proportional to the forward current flowing through it. If current through it changes the brightness also changes accordingly. To get a constant brightness the variation in the current flowing through LED should be constant. In other words the variation in the brightness is very small if the current change is small. In case 2 the variation in current is 10mA but it is only 1.46mA in case 1. Hence it can be concluded that the arrangement in case 1 is giving reasonably constant brightness. Therefore 24V supply in series with 820Ω resistor preferable for the constant brightness point of view from the LED.

03.

Sol: Given, wavelength = 500nm

(i) Work function of cathode(Ψ) = 1.2eV

(ii) Work function $h\theta_0 = 1.2 \times 1.6 \times 10^{-19}\text{ J}$
 $\Rightarrow h\theta - h\theta_0 = eV$

$$\Rightarrow \frac{hc}{\lambda} - 1.2 \times 1.6 \times 10^{-19} = eV$$

$$\Rightarrow \frac{6.625 \times 10^{-34} \times 3 \times 10^8}{500 \times 10^{-9}} - 1.2 \times 1.6 \times 10^{-19}$$

$$= 1.6 \times 10^{-19} \text{ V}$$

$$\Rightarrow V = 1.2843 \text{ Volts}$$

(iii) Given, anode voltage $V = 90 \text{ Volts}$

(iv) Wavelength $\lambda = 250 \text{ nm}$

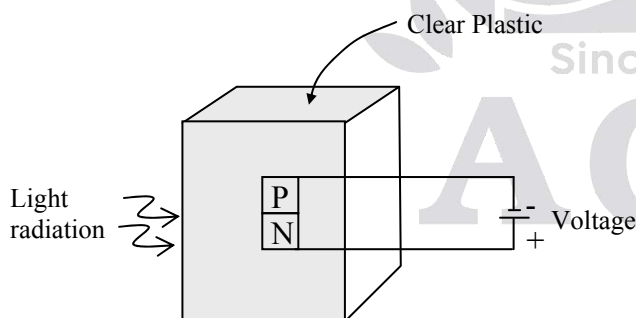
$$\text{Velocity} \Rightarrow v = \sqrt{\frac{2eV}{m}}$$

$$v = \sqrt{\frac{2 \times 1.6 \times 10^{-19} \times 90}{9.1 \times 10^{-31}}}$$

$$= 5.62 \times 10^6 \text{ m/sec}$$

04.

Sol: Photo diode is a reverse-biased p-n junction diode which is when illuminates, the current varies almost linearly with the light flux. This type of effect may be viewed in some p-n junction diode, which is known as PHOTO DIODE. It consist of a p-n junction is embedded in a clear plastic as shown in the figure below.



Radiation is allowed to fall upon one surface across the Junction. The remaining sides of the plastic are either painted black or enclosed in a metallic case.

Photo diode works on the principle of photo conductive effect.

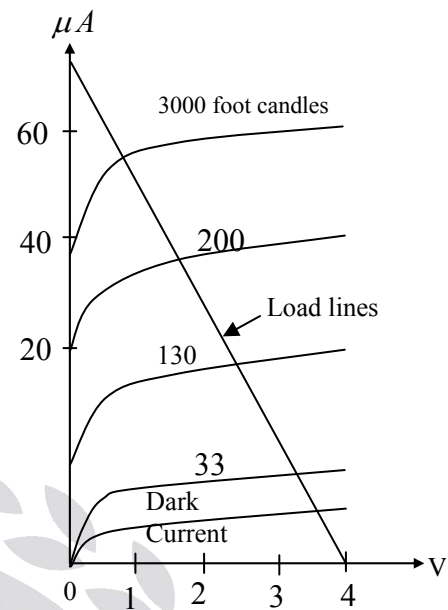


Fig: Volt – ampere characteristic of (Ge) photo diode

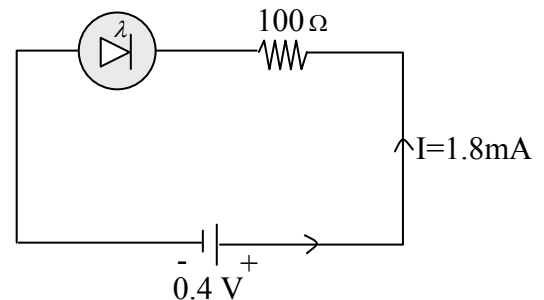
$$I = I_s + I_0 (1 - e^{V/\eta V_T})$$

Where, I_s = Short-circuit current and is proportional to the light intensity.

If the PN junction is open circuited, the light energy is used to create a potential difference which is proportional to the frequency and intensity of the incident light. This phenomenon works in photovoltaic converter.

If the light energy is used to change the resistance of PN diode which is proportional to the frequency and intensity of the incident light. This phenomenon works in photo resistor.

Now for numerical part,



Light intensity = 100 lm/cm^2

Let resistance offered by the photo diode
= $R \Omega$

$$\therefore 1.8 \times 10^{-3} A = \frac{0.4V}{R + 100} \Rightarrow R = 122.22 \Omega$$

We know that, $I_s \propto \text{Light intensity}$.

so, in the new case when light intensity is doubled then

$$(I_s)_{\text{new}} \approx 3.6 \times 10^{-3} A = \frac{0.4V}{R_{\text{new}} + 100}$$

$$R_{\text{new}} = 11.11 \Omega$$



Chapter 8

MOSFET

Objective Practice Solutions

01. Ans: (c)

Sol: $V_T = 1$

$$V_{DS} = 5 - 1 = 4 \text{ V}$$

$$V_{GS} = 3 - 1 = 2 \text{ V}$$

$$V_{GS} - V_T = 2 - 1 = 1 \text{ V}$$

$$V_{DS} > V_{GS} - V_T$$

$$4 > 1 \rightarrow \text{Saturation}$$

02. Ans: (d)

Sol: In active region (or) saturation region, channel is pinched off. Number of carriers present in the channel decreases from source end to drain end due to potential increases from source to drain.

03. Ans: (d)

$$\text{Sol: } \frac{I_{D2}}{I_{D1}} = \frac{K_n [V_{GS2} - V_T]^2}{K_n [V_{GS1} - V_T]^2}$$

$$\frac{I_{D2}}{1 \text{ mA}} = \frac{[1400 - 400]^2}{[900 - 400]^2}$$

$$I_{D2} = 4 \text{ mA}$$

04. Ans: (d)

$$\text{Sol: } A = 1 \text{ sq } \mu\text{m} = 10^{-12} \text{ m}^2$$

$$d = 1 \mu\text{m} = 1 \times 10^{-6} \text{ m}$$

$$N_D = 10^{19}/\text{cm}^3$$

$$n_i = 10^{10}$$

No. of holes = concentration $\times$ volume

$$\text{Volume} = A \times d = 10^{-18} \text{ m}^3$$

$$p = \frac{n_i^2}{n} = \frac{10^{20}}{10^{19}}$$

$$= 10 \text{ holes/cm}^3 = 10 \times 10^6 \text{ holes/m}^3$$

$$\therefore \text{No. of holes} = 10 \times 10^6 \times 10^{-18}$$

$$= 10^{-11} \text{ holes}$$

$$\approx 0$$

05. Ans: (b)

Sol: 1) since it has n-type source & drain, it is n-channel MOSFET.

2) Drain current flows only when $V_{GS} > 2\text{V}$, it implies it has threshold voltage (V_{th}) of +2V

$\Rightarrow$ It is enhancement type MOSFET.

$$3) V_{Th} = +2\text{V}$$

$$4) g_m = \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_{Th}]$$

transconductance depends upon electron mobility.

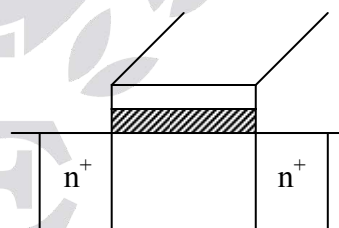
06. Ans: (b)

$$\text{Sol: } C_{sbo} = \frac{\epsilon_{si} A}{d}$$

$$d = 10 \text{ nm}$$

$$\epsilon_{si} = \epsilon_{rsi} \epsilon_0$$

$$= 11.7 \times 8.9 \times 10^{-12} \text{ F/m}$$



$$A = (0.2\mu \times 1\mu) + (0.2\mu \times 1\mu) + (0.2\mu \times 1\mu)$$

$$= 3(0.2\mu \times 1\mu) = 0.6 \times 10^{-12} \text{ m}^2$$

$$C_{sbo} = \frac{11.7 \times 8.9 \times 10^{-12} \times 0.6 \times 10^{-12}}{10 \times 10^{-9}}$$

$$C_{sbo} = 6.24 \times 10^{-15}$$

$$\approx 7 \text{ fF}$$

In practical IC, this cap will be provided to front and back sides also then area may be

$$A = (0.6 \times 10^{-12}) + (0.2 \mu \times 1 \mu) + (0.2 \mu \times 1 \mu)$$

$$A = 0.68 \times 10^{-12} \text{ m}^2$$

$$C_{sbo} = \frac{11.7 \times 8.9 \times 10^{-12} \times 0.68 \times 10^{-12}}{10 \times 10^{-9}} = 7 \text{ fF}$$

07. Ans: (a)

Sol: $L_{ov} = \delta = 20 \text{ nm}$

$$d = 10 \text{ nm}, w = 1 \mu\text{m}$$

$$\epsilon_{rsi} = 11.7, \epsilon_{rox} = 3.9$$

$$\epsilon_0 = 8.9 \times 10^{-12} \text{ F/m}$$

$$C_{ov} = C_{ox} w L_{ov} = \frac{\epsilon_{ox}}{t_{ox}} w L_{ov}$$

$$= \frac{\epsilon_{rox} \epsilon_0}{t_{ox}} w L_{ov}$$

$$= \frac{3.9 \times 8.9 \times 10^{-12} \times 1 \times 10^{-6} \times 20 \times 10^{-9}}{1 \times 10^{-9}}$$

$$= 0.69 \times 10^{-15} = 0.69 \text{ fF} \approx 0.7 \text{ fF}$$

08. Ans: (a)

Sol: $A = 1 \times 10^{-4} \text{ cm}^2$

$$\epsilon_{si} = 1 \times 10^{-12} \text{ F/cm}$$

$$\epsilon_{ox} = 3.5 \times 10^{-13} \text{ F/cm}$$

$$C_0 = 7 \text{ pF}$$

$$C_0 = C_{ox} A = \frac{\epsilon_{ox}}{t_{ox}} A$$

$$t_{ox} = \frac{\epsilon_{ox}}{C_0} A = \frac{3.5 \times 10^{-13} \times 1 \times 10^{-4}}{7 \times 10^{-12}}$$

$$= 5 \times 10^{-6} \text{ cm} = 50 \text{ nm}$$

09. Ans: (b)

Sol: $\frac{C_0 C_d}{C_0 + C_d} = 1 \text{ pF}$

$$\frac{7 C_d}{C_d + 7} = 1 \Rightarrow C_d = 7 \text{ pF}$$

$$C_d = C_{dep} A = \frac{\epsilon_{si}}{d} A$$

$$d = \frac{\epsilon_{si}}{C_d} A$$

$$= \frac{1 \times 10^{-12}}{\frac{7}{6} \times 10^{-12}} (1 \times 10^{-4}) \text{ cm} = 0.857 \mu\text{m}$$

10. Ans: (b)

Sol: $V_{Th} = 0.5 \text{ V}$

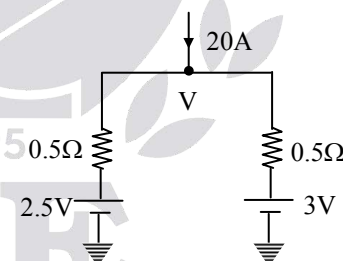
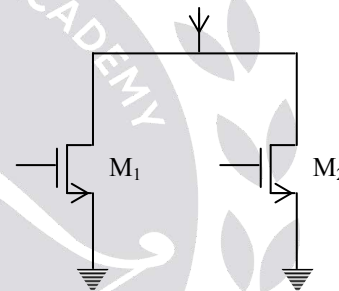
$$V_G = 3 \text{ V}$$

Pinch-off occurs when

$$V_D = V_G - V_{Th} = 3 - 0.5 = 2.5 \text{ V}$$

11. Ans: (a)

Sol:



$$20 = \frac{V - 2.5}{0.5} + \frac{V - 3}{0.5}$$

$$V = 7.75 \text{ Volts}$$

$$I_{D1} = \frac{7.75 - 2.5}{0.5} = 10.5 \text{ A}$$

$$I_{D2} = \frac{7.75 - 3}{0.5} = 9.5 \text{ A}$$

12. Ans: (b)

Sol: The input impedance of insulated gate MOSFET is very high because of SiO_2 layer and reverse bias at gate to source junction (i.e. at input junction).

Statement (II) also true but not the correct explanation of statement (I).

13. Ans: (d)

Sol: Statement (I) is false, for same drain current rating n-channel MOSFET occupies less area than p-channel MOSFET why because electron mobility is higher than hole mobility.

14. Ans: (a)

Sol: An Enhancement type MOSFET can be operate only in Enhancement mode. For n-channel EMOSFET, if V_{GS} (positive) $> V_{th}$, then only channel will formed between source and drain. So, for n-type EMOSFET only positive voltage can be applied to the gate with respect to the substrate. Therefore, statement-I is true.

Only with a positive voltage to the gate an "Inversion layer" is formed and conduction can take place. So statement-II is true and correct explanation of statement-I.

15. Ans: (b)

Sol: The drain current (I_D) of a MOSFET is controlled by the gate voltage. Therefore statement-I is true.

The input impedance for a MOSFET is very and the current through the gate terminal (I_G) is zero. Therefore, MOSFET is an insulated gate FET. So statement-II is true but not the correct explanation for statement-I.

Conventional Practice Solutions
01.

Sol: Transconductance, $g_m = \frac{\partial I_D}{\partial V_{DS}}$

$$= \frac{\mu_n C_{ox} W}{L} (V_{GS} - V_T)$$

Where,

C_{ox} = gate - oxide capacitance/ unit area

$$= \frac{\epsilon_0 \epsilon_x}{d_{ox}}$$

$$= \frac{3.9 \times 8.854 \times 10^{-12} \text{ F/m}}{2 \times 10^{-7} \text{ m}}$$

$$\therefore C_{ox} = 17.265 \times 10^{-5} \text{ F/m}^2$$

But in linear region,

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} V_{DS}$$

$$\Rightarrow g_m = \frac{0.08 \times 10^{-4} \times 17.265 \times 10^{-5}}{2 \times 10^{-6}} \times 1$$

$$= 0.6906 \times 10^{-3} \text{ mho}$$

$$g_m = 690 \mu \text{ mho}$$

02.

Sol: Given $\mu_n C_{ox} = \mu_p C_{ox} = 20 \mu \text{ A/V}^2$

$$W = 100 \mu \text{ m}, L = 10 \mu \text{ m}$$

$$I_{ref} = 100 \mu \text{ A}$$

When $\mu_n C_{ox} = \mu_p C_{ox}$

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} = \sqrt{2 \mu_p C_{ox} \frac{W}{L} I_D}$$

$$= \sqrt{2 \times 20 \times 10^{-6} \times \frac{100}{10} \times 100 \times 10^{-6}}$$

$$= 2 \times 10^{-4}$$

When early voltages for both P and n devices are equal i.e. $V_A = 100 \text{ V}$

$$R_L = R_D = \frac{V_A}{I_D} = \frac{100}{100 \times 10^{-6}} = 10^6$$

The small signal voltage gain

$$A_V = -g_m(R_D \parallel R_L)$$

$$= -g_m \frac{R_D R_L}{R_D + R_L} = -g_m \frac{R_D}{2}$$

$$= -2 \times 10^{-4} \times \frac{10^6}{2}$$

$$\approx -100$$

$$\therefore |A_V| = 100$$

03.

Sol: Case-1:

Given that, slope of I_D versus V_{GS} curve of an n-channel MOSFET in linear region is $10^{-3} \Omega^{-1}$

The drain current (I_D) in the linear region is given by

$$I_D = \mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\Rightarrow \frac{dI_D}{dV_{GS}} = \mu_n C_{ox} \left(\frac{W}{L} \right) V_{DS}$$

$$\Rightarrow \mu_n C_{ox} \left(\frac{W}{L} \right) V_{DS} = 10^{-3}$$

$$\therefore \frac{dI_D}{dV_{GS}} = \text{slope} = 10^{-3} \Rightarrow \text{given}$$

$$\Rightarrow \mu_n C_{ox} \left(\frac{W}{L} \right) = \frac{10^{-3}}{V_{DS}}$$

$$\Rightarrow \mu_n C_{ox} \left(\frac{W}{L} \right) = 10 \times 10^{-3} \quad \because V_{DS} = 0.1 \text{ volt}$$

$$\Rightarrow \text{given} \quad \text{----- (1)}$$

Case-2

The drain current for as n-channel MOSFET in saturation region is express as

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \quad (\text{neglecting}$$

channel length modulation)

$$\sqrt{I_D} = \sqrt{\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2}$$

$$\therefore \frac{d\sqrt{I_D}}{dV_{GS}} = \sqrt{\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)}$$

$$\Rightarrow \frac{d\sqrt{I_D}}{dV_{GS}} = \sqrt{\frac{1}{2} \times 10 \times 10^{-3}}$$

$$\left[\because \mu_n C_{ox} \left(\frac{W}{L} \right) = 10 \times 10^{-3} \right]$$

$$\Rightarrow \frac{d\sqrt{I_D}}{dV_{GS}} = 70.71 \times 10^{-3} \frac{\sqrt{A}}{V}$$

$\therefore$ Slope of the $\sqrt{I_D}$ versus V_{GS} curve under saturation region is $70.71 \times 10^{-3} \frac{\sqrt{A}}{V}$.

Chapter 9

Biassing

Objective Practice Solutions

Biassing

01. Ans: (c)

$$\text{Sol: } R_D = \frac{V_{DD} - V_D}{I_D} = \frac{20V - 12V}{2.5mA} = 3.2 K\Omega$$

In self bias

$$V_{GS} = -I_D R_S$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$V_{GS} = V_p \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

$$V_{GS} = -1.06 V$$

$$R_S = \frac{V_{GS}}{-I_D} = \frac{-1}{-2.5} = 400 \Omega$$

02. Ans: (b)

$$\text{Sol: } V_G = V_{GS} + I_D R_S$$

$$I_D = \frac{16-8}{1.8K} = 4.4mA$$

$$V_G = \frac{16 \times 47}{138} = 5.45 V$$

$$R_S = \frac{V_G - V_{GS}}{I_D} = \frac{5.4 - (-2V)}{4.4mA} = 1.68K\Omega$$

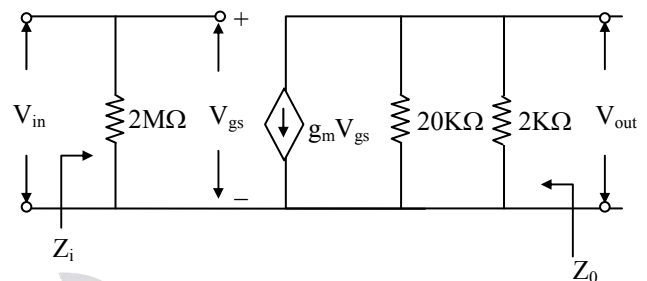
03. Ans: (c)

$$\text{Sol: } V_{DS} = V_{DD} - I_D(R_D + R_S) \\ = 30 V - 4 mA(3.3K + 1.5K)$$

$$V_{DS} = 10.8 V$$

04. Ans: (b)

Sol: AC analysis,



$$Z_i = 2M\Omega,$$

$$Z_o = 20K\Omega \parallel 2K\Omega$$

$$\Rightarrow Z_o = \frac{20}{11} K\Omega$$

05. Ans: (a)

$$\text{Sol: } I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

$$= 10 \times 10^{-3} \left[1 - \frac{-2}{-8} \right]^2 = 5.625mA$$

KVL at output loop,

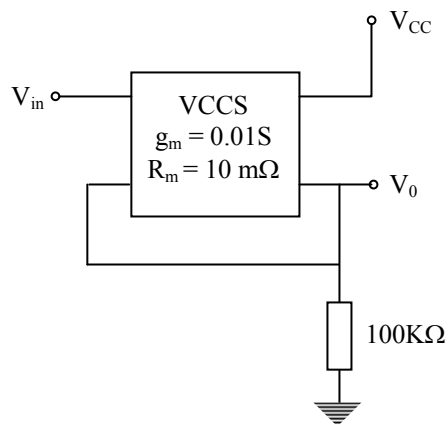
$$-20 + (2 \times 10^3 I_D) + V_{DS} = 0$$

$$V_{DS} = 20 - (2 \times 10^3 \times 5.625 \times 10^{-3}) \\ = 8.75V$$

06. Ans: (b) (By Printing Mistake in Volume-I Answer (c) is wrong, Correct answer is (b))

Sol: By observing,

The circuit is common drain i.e., source follower circuit.



$$R_o = r_d \parallel R_s \parallel \frac{1}{g_m}$$

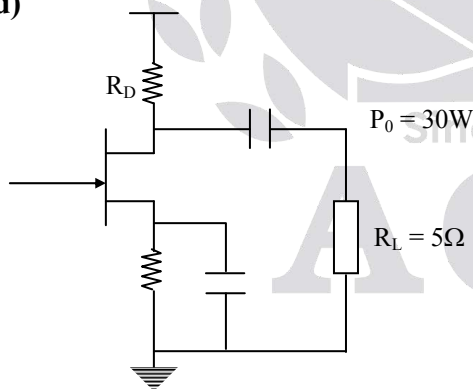
$$= 10 \text{ M}\Omega \parallel 100 \text{ K}\Omega \parallel 100 \Omega$$

$$= 100 \Omega$$

FREQUENCY ANALYSIS

01. Ans: (d)

Sol:



$$P_0 = \frac{V_o^2}{R_L}$$

$$30 \times 5 = V_o^2$$

$$V_o = 12.25 \text{ V}$$

$$A_v = \frac{V_o}{V_i}$$

$$A_v (\text{dB}) = 20 \log_{10} A_v$$

$$20 = 20 \log_{10} A_v$$

$$A_v = 10^1 = 10$$

$$\frac{V_o}{V_i} = 10$$

$$V_i = \frac{V_o}{10} = \frac{12.25}{10} \text{ V} = 1.225 \text{ V}$$

02. Ans: (b)

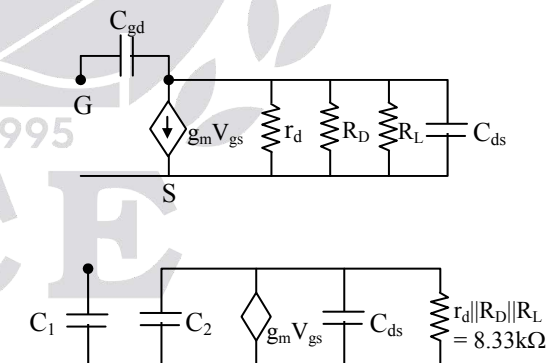
Sol: $A_v (\text{dB}) = 20 \log_{10} A_v$

$$50 = 20 \log_{10} A_v$$

$$A_v = 10^{(5/2)} = 316.228$$

03. Ans: $6.123 \times 10^6 \text{ Hz}$

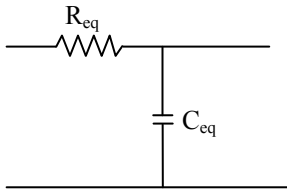
Sol: Small signal equivalent



$$C_2 = C_{gd} \left(1 - \frac{1}{A_v} \right),$$

$A_v = \text{mid-band,}$

$$\text{gain} = g_m(r_d \parallel R_D \parallel R_L) = -16.66$$



$$C_2 = 2\text{pF} \left(1 - \frac{1}{-16.66} \right) = 2.12 \text{ pF}$$

$$f_H = \frac{1}{2\pi C_{eq} R_{eq}}$$

$$C_{eq} = 1 + 2.12 = 3.12 \text{ pF}, R_{eq} = 8.33\text{k}\Omega$$

$$\Rightarrow f_H = 6.123 \times 10^6 \text{ Hz}$$

MOSFET BIASING

01. Ans: (b)

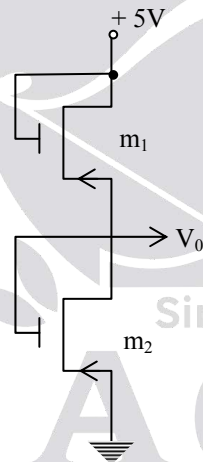
Sol: $V_T = 0.8$

$$K_n = 30 \times 10^{-6}$$

$$\left(\frac{W_1}{L} \right)_1 = \left(\frac{W}{L} \right)_2 = 40$$

$$V_{D_1} = +5$$

$$I_{D_1} = I_{D_2}$$



$$\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{GS_1} - V_T)^2$$

$$= \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_2 (V_{GS_2} - V_T)^2$$

$$V_{GS_1} = V_{D_1} - V_0$$

$$= +5 - V_0$$

$$V_{GS_2} = V_{G_1} - V_S = V_0 - 0 = V_0$$

$$\left(\frac{W}{L} \right)_1 (5 - (V_0) - 0.8)^2 = \left(\frac{W}{L} \right)_2 (V_0 - 0.8)^2$$

$$V_0 = 2.5\text{V}$$

02. Ans: (a)

Sol: $\left(\frac{W}{L} \right)_1 (V_{GS_1} - V_T)^2 = \left(\frac{W}{L} \right)_2 (V_{GS_2} - V_T)^2$

$$40 (4.2 - V_0)^2 = 15 (V_0 - 0.8)^2$$

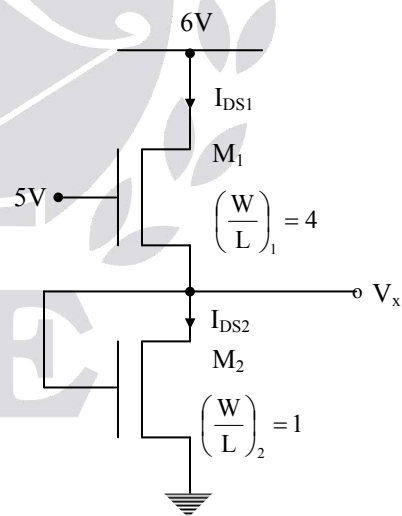
$$V_0 = 2.91 \text{ V}$$

03. Ans: (c)

Sol: From figure $I_{DS1} = I_{DS2}$.

$$\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{GS_1} - V_t)^2$$

$$= \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_2 (V_{GS_2} - V_t)^2$$



$$\therefore 4(5 - V_x - V_t)^2 = 1(V_x - V_t)^2$$

$$(\because V_{GS1} = V_G - V_x = 5 - V_x)$$

$$\Rightarrow 2(5 - V_x - V_t) = (V_x - V_t)$$

$$\therefore V_x = 3\text{V}$$

04. Ans: (d)

Sol:
$$\frac{V_2}{V_i} = \frac{g_m R_s}{1 + g_m R_s} \text{ ---- (1)}$$

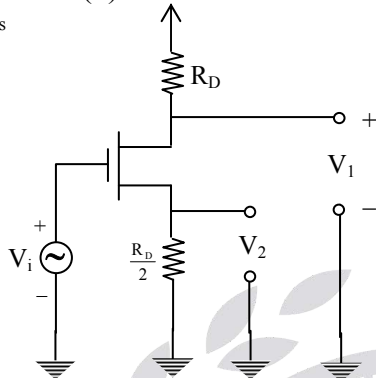
$$\frac{V_1}{V_i} = \frac{-g_m R_D}{1 + g_m R_s} \text{ ---- (2)}$$

(1) ÷ (2) ⇒

$$\frac{V_2}{V_1} = \frac{R_s}{-R_D}$$

$$\frac{V_2}{V_1} = \frac{-1}{2}$$

$$V_1 = -2V_2$$



Conventional Practice Solutions

01.

Sol: Apply KVL in loop (1)

$$1000 I_G + V_{GS} + 0.5 I_{DS} = 0$$

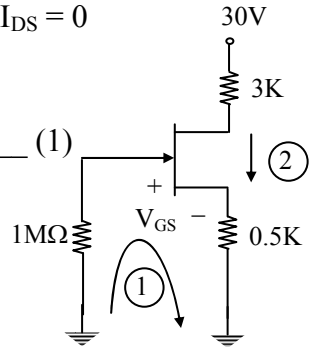
(I_G is negligible)

$$V_{GS} = -0.5 I_{DS}$$

$$I_{DS} = -2V_{GS} \text{ ---- (1)}$$

Given equation,

$$I_D = 16 \left[1 + \frac{V_{GS}}{4} \right]^2$$



$$\Rightarrow -2V_{GS} = 16 \left[1 + \frac{V_{GS}^2}{16} + \frac{V_{GS}}{2} \right]$$

$$-2V_{GS} = 16 + V_{GS}^2 + 8V_{GS}$$

$$V_{GS}^2 + 10V_{GS} + 16 = 0 \Rightarrow V_{GS} = -2 \text{ (or) } -8$$

V_{GS} should lie between 0 to V_P

(i.e. $V_P = -4V$) $\therefore V_{GS} = -2V$

Apply KVL to loop (2)

$$-30 + 3I_{DS} + V_{DS} + 0.5I_{DS} = 0$$

$$V_{DS} = 30 - 3.5I_{DS}$$

$$\Rightarrow V_{DS} = 30 - 3.5 \times 2 \times 2$$

$$\Rightarrow V_{DS} = 16V$$

From (1) $\Rightarrow I_D = -2 \times (-2V) \text{ mA}$

$$I_D = 4\text{mA}$$

02.

Sol: Given data

$$V_{TN} = 1V$$

$$K = 0.8 \times 10^{-3} \text{ A/V}^2$$

(i) For saturation region

$$I_D = k[V_{GS} - V_{TN}]^2$$

$$\Rightarrow I_D = 0.8 \times 10^{-3} [V_G - V_S - 1]^2$$

$$\Rightarrow I_D = 0.8 \times 10^{-3} [2.1 - 1]^2$$

$$(V_G = 2.1V, V_S = 0V)$$

$$\Rightarrow I_D = 0.968\text{mA}$$

$$\Rightarrow I_D \approx 1\text{mA}$$

(ii) Transconductance, $g_m = \frac{2I_D}{(V_{GS} - V_T)}$

$$\Rightarrow g_m = \frac{2 \times 10^{-3}}{(2.1 - 1)}$$

$$\Rightarrow g_m = 1.81 \text{ mA/V}$$

(iii) For $V_i = 10 \text{ mV}$

$$V_{GS} = 2.1 + (10 \times 10^{-3})$$

$$\Rightarrow V_{GS} = 2.11 \text{ Volts}$$

$$\therefore I_D = K[V_{GS} - V_{TN}]^2$$

$$\Rightarrow I_D = 0.8 \times 10^{-3} [2.11 - 1]^2$$

$$\Rightarrow I_D = 9.8568 \times 10^{-4} \text{ A}$$

$$\therefore I_D = 0.98568 \text{ mA}$$

$$\text{Drain voltage, } V_0 = V_{DD} - I_D R_D$$

$$\Rightarrow V_0 = 9 - (9.8568 \times 10^{-3} \times 2 \times 10^3)$$

$$\Rightarrow V_0 = 7.0288 \text{ Volts}$$

For saturation region

$$I_D = K[V_{GS} - V_{Th}]^2$$

$$\Rightarrow K = \frac{I_D}{(V_{GS} - V_{Th})^2}$$

$$\Rightarrow K = \frac{0.5 \times 10^{-3}}{(1.6 - 0.8)^2} (\because V_{GS} = V_{DS} = V_D)$$

$$\Rightarrow K = 7.8125 \times 10^{-4} \text{ A/V}^2$$

For $V_D = 2 \text{ Volts}$

$$I_D = K[2 - 0.8]^2$$

$$\Rightarrow I_D = 7.8125 \times 10^{-4} [2 - 0.8]^2$$

$$\Rightarrow I_D = 1.125 \text{ mA}$$

$\therefore$ The new value of I_D is 1.125mA

03.

Sol:

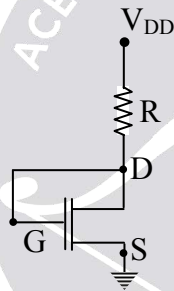
Given data

$$V_{Th} = 0.8 \text{ V}$$

$$V_D = 1.6 \text{ V}$$

$$I_D = 0.5 \text{ mA}$$

As, $V_{DS} = V_{GS} \Rightarrow$ MOSFET is always in saturation region for saturation region



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Chapter 10 CMOS & Device Technology

Objective Practice Solutions

01. Ans: (c)

Sol: $\overline{A(B+C)+DE}$

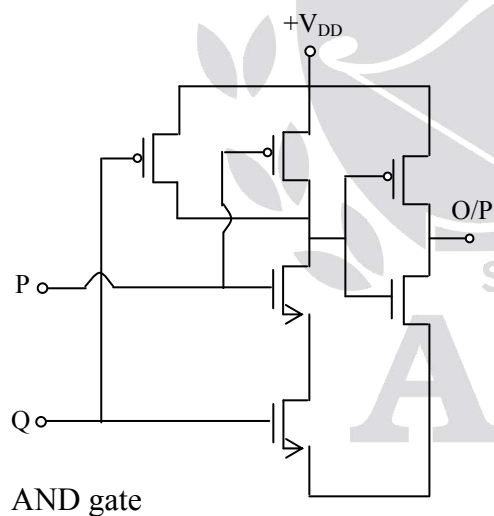
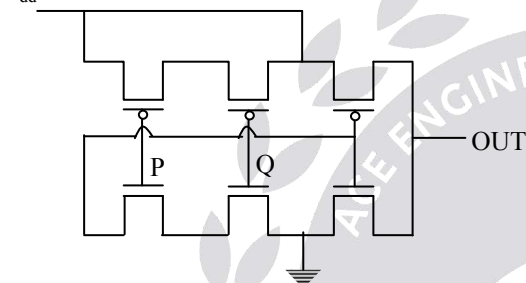
After option (c) as above answer

02. Ans: (a)

Sol: $\overline{X_1 + X_2}$

03. Ans: (d)

Sol: V_{dd}



04. Ans: (b)

Sol: $n = \frac{1}{2Nf}$

$$n = \frac{1}{2 \times 5 \times 10^6} = 10^{-8} \text{ sec} = 10 \text{ nsec}$$

Device Technology Key

01. (c) 02. (b) 03. (d)

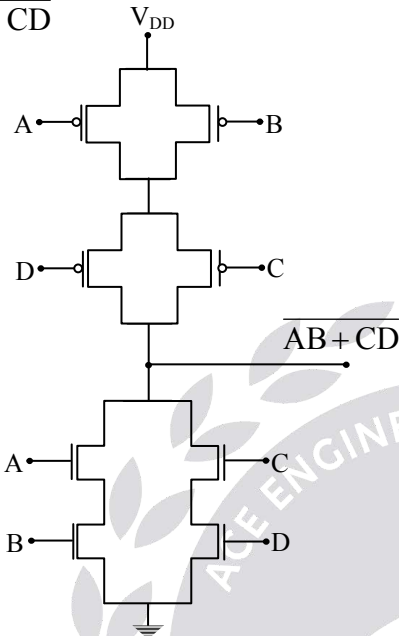
04. (b) 05. (a)

Conventional Practice Solutions

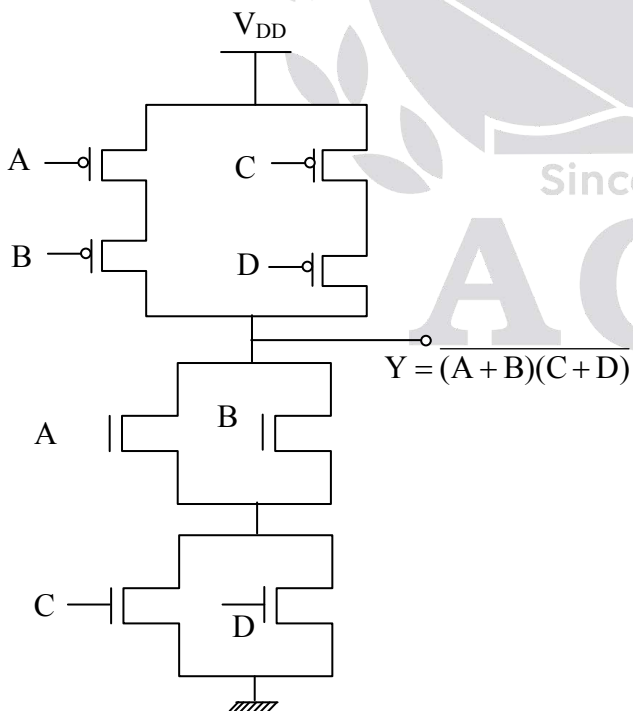
01.

Sol:

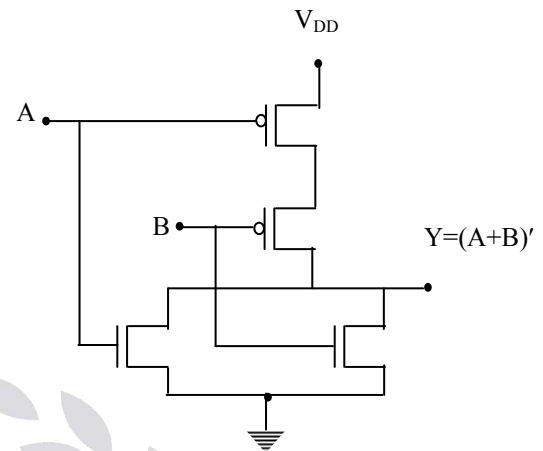
(a) $Y = \overline{AB + CD}$



(b) $Y = \overline{(A + B)(C + D)}$



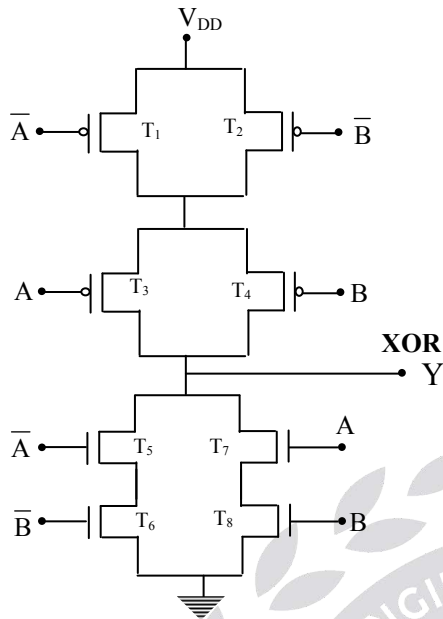
(c) $Y = \overline{A + B}$



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

In order to design CMOS circuit we require one N-channel MOSFET and one P-channel MOSFET. N-channel in series represents OR operation. As the NOR gate contains 2 inputs so we require four MOSFETS. When all inputs are Low N-channel transistors are OFF P-channel transistors are ON. Then output is V_{DD} = Logic1, If any input is high P-channel transistors are OFF, N-channel transistors are ON. O/p is Low i.e. Logic '0'.

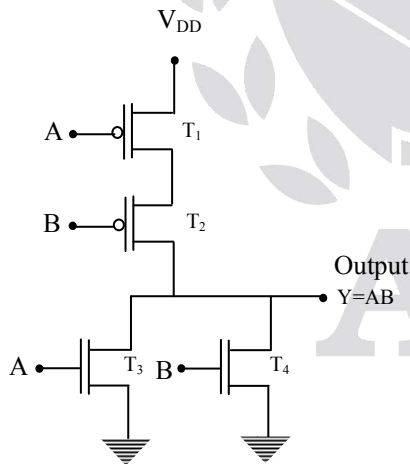
(d) 2-input XOR gates using CMOS:



Truth Table:

A	B	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆	T ₇	T ₈	Y
0	0	OFF	OFF	ON	ON	ON	ON	OFF	OFF	0
0	1	OFF	ON	ON	OFF	ON	OFF	OFF	ON	1
1	0	ON	OFF	OFF	ON	OFF	ON	ON	OFF	1
1	1	ON	ON	OFF	OFF	OFF	OFF	ON	ON	0

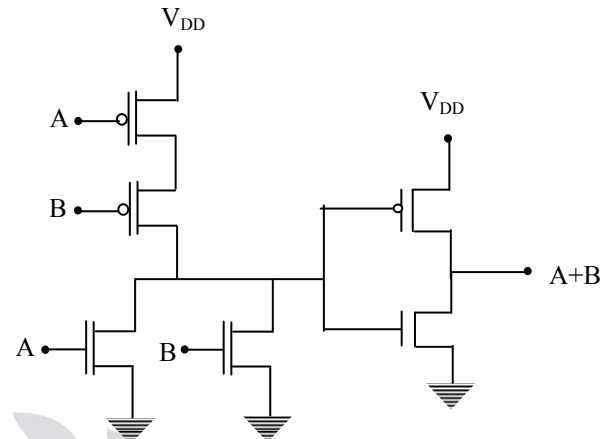
(e) $Y = AB$



Truth Table:

A	B	T ₁	T ₂	T ₃	T ₄	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

(f) $Y = A + B$



02.

Sol: An integrated circuit or monolithic integrated circuit (also referred to as IC, chip, or microchip) is an electronic circuit manufactured by the patterned diffusion of trace elements into the surface of a thin substrate of semiconductor material. Additional materials are deposited and patterned to form interconnections between semiconductor devices.

Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. Computers, mobile phones, and other digital appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of production of integrated circuits.

Among the most advanced integrated circuits are the microprocessors or "cores", which control everything from computers and cellular phones to digital microwave ovens. Digital memory chips and ASICs are examples of other families of integrated circuits that are important to the modern information society.

Merits or Advantages of Integrated Circuits:

The integrated circuits offer a number of advantages over those made by interconnecting discrete components. These are summarized as follows:

1. Extremely small size-thousands times smaller than discrete circuit. It is because of fabrication of various circuit elements in a single chip of semi-conductor material.
2. Very small weight owing to miniaturized circuit.
3. Very low cost because of simultaneous production of hundreds of similar circuits on a small semiconductor wafer. Owing to mass production an IC costs as much as an individual transistor.
4. More reliable because of elimination of soldered joints and need for fewer inter-connections.
5. Low power consumption because of their smaller size.
6. Easy replacement as it is more economical to replace them than to repair them.
7. Increased operating speeds because of absence of parasitic capacitance effect.
8. Close matching of components and temperature coefficients because of bulk production in batches.
9. Improved functional performance as more complex circuits can be fabricated for achieving better characteristics.
10. Greater ability of operating at extreme temperatures.
11. Suitable for small signal operation because of no chance of stray electrical pickup as various components of an IC is located very close to each other on a silicon wafer.
12. No component project above the chip surface in an IC as all the components are formed within the chip.

Demerits or Disadvantages of Integrated Circuits

The integrated circuits have few limitations also, as listed below:

1. In an IC the various components are part of a small semi-conductor chip and the individual component or components cannot be removed or replaced, therefore, if any component in an IC fails, the whole IC has to be replaced by the new one.
2. Limited power rating as it is not possible to manufacture high power (say greater than 10 Watt) ICs.
3. Need of connecting inductors and transformers exterior to the semi-conductor chip as it is not possible to fabricate inductors and transformers on the semi-conductor chip surface.
4. Operations at low voltage as ICs function at fairly low voltage.
5. Quite delicate in handling as these cannot withstand rough handling or excessive heat.
6. Need of connecting capacitor exterior to the semi-conductor chip as it is neither convenient nor economical to fabricate capacitances exceeding 30 pF. Therefore, for higher values of capacitance, discrete components exterior to IC chip are connected.
7. High grade P-N-P assembly is not possible.
8. Low temperature coefficient is difficult to be achieved.
9. Difficult to fabricate an IC with low noise.
10. Large value of saturation resistance of transistors.

11. Voltage dependence of resistors and capacitors.
12. The diffusion processes and other related procedures used in the fabrication process are not good enough to permit a precise control of the parameter values for the circuit elements. However, control of the ratios is at a sufficiently acceptable level.

Fabrication of monolithic ICs is the most complex aspect of microelectronic devices. There are two types of monolithic fabrication method. These are the **DIFFUSION METHOD** and the **EPITAXIAL METHOD**.

DIFFUSION METHOD:

The **DIFFUSION** process begins with the highly polished silicon wafer being placed in an oven (figure-1). The oven contains a concentration impurity made up of impurity atoms which yield the desired electrical characteristics. The concentration of impurity atoms is diffused into the wafer and is controlled by controlling the temperature of the oven and the time that the silicon wafer is allowed to remain in the oven. This is called **DOPING**. When the wafer has been uniformly doped, the fabrication of semiconductor devices may begin. Several hundred circuits are produced simultaneously on the wafer.

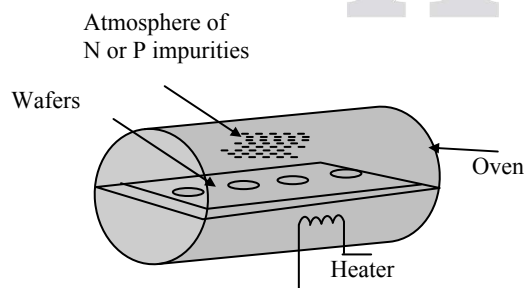


Figure: 1 Wafers in a diffusion oven.

EPITAXIAL METHOD:

The **EPITAXIAL** process involves depositing a very thin layer of silicon to form a uniformly doped crystalline region (epitaxial layer) on the substrate. Components are produced by diffusing appropriate materials into the epitaxial layer in the same way as the planar-diffusion method. When planar-diffusion and epitaxial techniques are combined, the component characteristics are improved because of the uniformity of doping in the epitaxial layer. A cross section of a typical planar-epitaxial transistor is shown in fig 2. Note that the component parts do not penetrate the substrate as they did in the planar-diffused transistor.

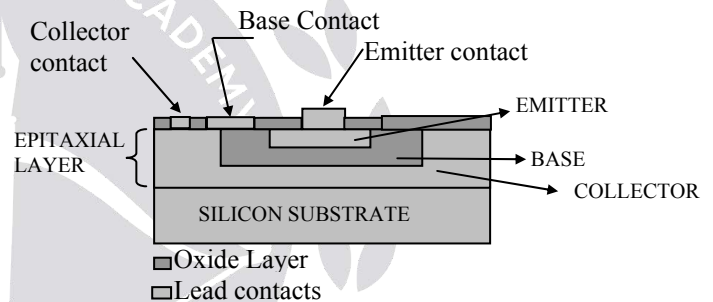


Fig. 2: Planar-epitaxial transistor