GATE | PSUs

ELECTRICAL ENGINEERING
Digital Electronics and Microprocessors

Text Book: Theory with worked out Examples and Practice Questions
1. Number Systems

01. Ans: (d)
Sol: \[135x + 144x = 323x\]
\[(1\times x^2 + 3 \times x^1 + 5 \times x^0)+(1\times x^2+4x^1+ 4x^0)\]
\[= 3x^2 + 2x^1 + 3x^0\]
\[\Rightarrow x^2+3x+5+x^2+4x+4 = 3x^2+ 2x + 3\]
\[x^2 - 5x - 6 = 0\]
\[(x-6) (x+ 1) = 0\] (Base cannot be negative)
Hence \(x = 6\).

02. Ans: (a)
Sol: 8-bit representation of 
\[+127_{10} = 01111111_{(2)}\]
1’s complement representation of 
\[– 127 = 10000000.\]
2’s complement representation of 
\[– 127 = 10000001.\]
No. of 1’s in 2’s complement of 
\[– 127 = m = 2\]
No. of 1’s in 1’s complement of 
\[– 127 = n = 1\]
\[\therefore m: n = 2:1\]

03. Ans: (c)
Sol: In 2’s complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is ‘X3’, hence it can be extended left any number of times.

04. Ans: (c)
Sol: Binary representation of \((+539)_{10}\):

\[
\begin{array}{c|c|c|c|c|c|c|c|c|c}
& & & & & & & & & \\
0 & 2 & 5 & 3 & 9 & & & & & \\
2 & 2 & 6 & 9 & -1 & & & & & \\
2 & 1 & 3 & 4 & -1 & & & & & \\
2 & 6 & 7 & -0 & & & & & & \\
2 & 3 & 3 & -1 & & & & & & \\
2 & 1 & 6 & -1 & & & & & & \\
2 & 8 & -0 & & & & & & & \\
2 & 4 & -0 & & & & & & & \\
2 & 2 & -0 & & & & & & & \\
1 & -0 & & & & & & & & \\
\end{array}
\]
\[(+539)_{10} = (10000 11 0 11) = (00100 0011011)_{2}\]
2’s complement \[\rightarrow 110111100101\]
Hexadecimal equivalent \[\rightarrow (DE5)_{H}\]

05. Ans: 5
Sol: Symbols used in this equation are 0,1,2,3
Hence base or radix can be 4 or higher
\[3x^2 + 1x +2x^0 = (2x+0) \times (x+3x^0+x^{-1})\]
\[3x^2+x+2 = (2x) \left( x + 3 + \frac{1}{x} \right)\]
\[3x^2 + x + 2 = 2x^2 + 6x + 2\]
\[x^2 - 5x = 0\]
\[x(x -5) = 0\]
x = 0 (or) x = 5
x must be x > 3, So x = 5

06. Ans: 3
Sol: 1235 = x8y
1 × 52 + 2 × 51 + 3 × 50 = x.y \( \overline{x} \) + 8 × \( \overline{y} \)
25 + 10 + 3 = xy + 8
\( \therefore \) xy = 30
Possible solutions:
i. x = 1, y = 30
ii. x = 2, y = 15
iii. x = 3, y = 10
\( \therefore \) 3 possible solutions exists.

07. Ans: 1
Sol: The range (or) distinct values
For 2’s complement \( \Rightarrow -(2^{n-1}) \) to \( +(2^{n-1}-1) \)

For sign magnitude
\( \Rightarrow -(2^{n-1}-1) \) to \( +(2^{n-1}-1) \)

Let n = 2 \( \Rightarrow \) in 2’s complement
\( -(2^{2-1}) \) to \( +(2^{2-1}-1) \)
\( -2 \) to +1 \( \Rightarrow -2, -1, 0, +1 \) \( \Rightarrow X = 4 \)
n = 2 in sign magnitude \( \Rightarrow -1 \) to +1 \( \Rightarrow Y = 3 \)
X – Y = 1

2. Logic Gates & Boolean Algebra

01. Ans: (c)
Sol: Given 2’s complement numbers of sign bits are x & y. z is the sign bit obtained by adding above two numbers. \( \therefore \) Overflow is indicated by \( = \overline{x} \overline{y} \overline{z} + x y z \)

02. Ans: (b)
Sol: Truth table of XOR

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>o/p</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Stage 1:
Given one i/p = 1 Always.

1 X o/p
-----------
1 0 1 = \( \overline{X} \)
1 1 0 = \( \overline{X} \)

For First XOR gate o/p = \( \overline{X} \)

Stage 2:

\( \overline{X} \) X o/p
-----------
0 1 1
1 0 1
For second XOR gate o/p = 1.
Similarly for third XOR gate o/p = \( \overline{X} \) & for fourth o/p = 1
For Even number of XOR gates o/p = 1
For 20 XOR gates cascaded o/p = 1.

**03.** Ans: (b)
Sol:

\[
\begin{align*}
\text{Number of min terms} &= 20
\end{align*}
\]

**04.** Ans: (c)
Sol:

\[
\begin{align*}
x &= f_1f_2 \\
f_4 &= f_1f_2 + f_3 \\
f_2 &= \sum m(6, 8)
\end{align*}
\]

**05.** Ans: (d)
Sol:

\[
\begin{align*}
M(a, b, c) &= ab + bc + ca \\
M(a, b, c) &= \overline{bc} + \overline{a}b + \overline{a}c \\
M(a, b, c) &= ab + \overline{bc} + \overline{a}c \\
M(a, b, c) &= \sum m(1, 2, 4, 7)
\end{align*}
\]

\[
\begin{align*}
\therefore \ M(x, y, z) &= a \oplus b \oplus c \\
\text{Where} \ x &= M(a, b, c), \ y = M(a, b, c), \ z = c
\end{align*}
\]
08. Ans: 40

Sol:

\[ f = \overline{x}z + x\overline{z} \]

09. Ans: (c)

Sol: Logic gates \( \overline{X} + Y = \overline{XY} = XY_1 \)

Where \( Y_1 = \overline{Y} \)

It is a NAND gate and thus the gate is ‘Universal gate’.


01. Ans: (b)

Sol:

\[ f = xy + yw \]

POS: \( y(x+y) \)

02. Ans: (b)

Sol: \( f = \overline{b} \overline{d} + \overline{b} \overline{c} \)

03. Ans: (b)

Sol: \( f = xy + yw \)

POS: \( y(x+y) \)

04. Ans: (a)

Sol: For n-variable Boolean expression,

Maximum number of minterms = \( 2^n \)

Maximum number of implicants = \( 2^n \)

Maximum number of prime implicants = \( \frac{2^n}{2} = 2^{n-1} \)
05. Ans: (c)  
Sol:  
\[
\begin{array}{c|c|c|c} 
A & B & C & F(A, B, C)  \\
0 & 0 & 0 & 0  \\
0 & 0 & 1 & 0  \\
0 & 1 & 0 & 1  \\
0 & 1 & 1 & 0  \\
1 & 0 & 0 & 1  \\
1 & 0 & 1 & 0  \\
1 & 1 & 0 & 0  \\
1 & 1 & 1 & 1  \\
\end{array}
\]

\[F(A, B, C) = \overline{AC} + BC\]

06. Ans: 1  
Sol: After minimization = \((\overline{A} + B + \overline{C} + D)\)  
= ABCD  
∴ Only one minterm.

07. Ans: 3  
Sol:  
\[
\begin{align*}
W & = \overline{w}z + \overline{w}xy + x\overline{y}z  \\
\text{Total number of prime implicants of the function ‘f’} & = 3
\end{align*}
\]

4. Combinational Circuits

01. Ans: (d)  
Sol: Let the output of first MUX is “F1”  
\[F_1 = A I_0 + A I_1\]  
Where A is selection line, I_0, I_1 = MUX Inputs  
\[F_1 = S_i \cdot W + S_i \cdot \overline{W} = S_i \oplus W\]  
Output of second MUX is  
\[F = \overline{A} I_0 + A I_1\]  
\[F = S_2 \cdot F_1 + S_2 \cdot \overline{F_1}\]  
\[F = S_2 \oplus F_1\]  
But \(F_1 = S_1 \oplus W\)  
\[F = S_2 \oplus S_1 \oplus W\]  
i.e., \(F = W \oplus S_1 \oplus S_2\)

02. Ans: 50  
Sol:  
Initially all the output values are ‘0’, at \(t = 0\), the inputs to the 4-bit adder are changed to \(X_3X_2X_1X_0 = 1100, Y_3Y_2Y_1Y_0 = 0100\)  
- - - - - - indicates critical path delay to get the output
i.e. critical time (or) maximum time is taken for \( Z_4 \) to get final output as ‘1’

\[ \begin{align*}
\text{Z}_0 &= 1 \\
\text{Z}_1 &= 0 \\
\text{Z}_2 &= 0 \\
\text{Z}_3 &= 0 \\
\text{Z}_4 &= 0 \rightarrow 1 \\
\end{align*} \]

Total time taken = \( \Delta t_1 + \Delta t_2 = 50 \) ns

i.e. critical time (or) maximum time is taken for \( Z_4 \) to get final output as ‘1’
03. Ans: (a)

<table>
<thead>
<tr>
<th>K</th>
<th>C&lt;sub&gt;0&lt;/sub&gt;</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A+B (addition)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>A+B+1 (addition with carry)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A+\overline{B} (1’s complement addition)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A+\overline{B}+1 (2’s complement subtraction)</td>
</tr>
</tbody>
</table>

04. Ans: (d)
Sol: It is expansion of 2:4 decoders to 1:8 demultiplexer A<sub>1</sub>, A<sub>0</sub> must be connected to S<sub>1</sub>, S<sub>0</sub> i.e., R = S<sub>0</sub>, S = S<sub>1</sub>
Q must be connected to S<sub>2</sub> i.e., Q = S<sub>2</sub>
P is serial input must be connected to D<sub>in</sub>

05. Ans: 6
Sol: T = 0 → NOR → MUX 1 → MUX 2
2ns 1.5ns 1.5ns
Delay = 2ns + 1.5ns + 1.5ns = 5ns
T = 1 → NOT → MUX 1→NOR→ MUX 2
1ns 1.5ns 2ns 1.5ns
Delay = 1ns + 1.5ns + 2ns + 1.5ns = 6ns
Hence, the maximum delay of the circuit is 6ns

06. Ans: –1
Sol: When all bits in ‘B’ register is ‘1’, then only it gives highest delay.
∴ ‘–1’ in 8 bit notation of 2’s complement is 1111 1111

5. Sequential Circuits

01. Ans: (c)
Sol: Given Clk, X<sub>1</sub>, X<sub>2</sub>
Output of First D-FF is Q<sub>1</sub>
Output of Second D-FF is Q<sub>2</sub>

02. Ans: 4
Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

03. Ans: 7
Sol: The counter is cleared when
Q<sub>D</sub>Q<sub>C</sub>Q<sub>B</sub>Q<sub>A</sub> = 0110

<table>
<thead>
<tr>
<th>Clk</th>
<th>Q&lt;sub&gt;D&lt;/sub&gt;</th>
<th>Q&lt;sub&gt;C&lt;/sub&gt;</th>
<th>Q&lt;sub&gt;B&lt;/sub&gt;</th>
<th>Q&lt;sub&gt;A&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get’s cleared during the 7th clock pulse.
∴ mod of counter = 7

04. Ans: (b)
Sol: The given circuit is a mod 4 ripple down counter. Q₁ is coming to 1 after the delay of 2Δt.

<table>
<thead>
<tr>
<th>CLK</th>
<th>Q₁ Q₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0</td>
</tr>
<tr>
<td>1</td>
<td>1 1</td>
</tr>
<tr>
<td>2</td>
<td>1 0</td>
</tr>
<tr>
<td>3</td>
<td>0 1</td>
</tr>
<tr>
<td>4</td>
<td>0 0</td>
</tr>
</tbody>
</table>

05. Ans: (c)
Sol: Assume n = 2

clk → 2-bit counter → Q₁ → 2x4 decoder → Q₀

Outputs of counter is connected to inputs of decoder

06. Ans: (b)
Sol:

<table>
<thead>
<tr>
<th>CLK</th>
<th>Serial in= B ⊕ C ⊕ D</th>
<th>A  B  C  D</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1 1 0 1</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>1</td>
<td>1 1 0 1</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>2</td>
<td>1 0 1 0</td>
<td>0 0 1 1</td>
</tr>
<tr>
<td>3</td>
<td>0 0 1 1</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>4</td>
<td>0 0 1 1</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>5</td>
<td>1 1 0 0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>6</td>
<td>0 1 0 0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>7</td>
<td>1 0 1 0</td>
<td>0 0 0 0</td>
</tr>
</tbody>
</table>

∴ After 7 clock pulses content of shift register become 1010 again.

07. Ans: (b)
Sol:

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>( \bar{Q}_n )</th>
<th>( T = \left( J + Q_n \right) \left( K + \bar{Q}_n \right) )</th>
<th>( Q_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.1 = 0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.0 = 0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0.1 = 0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1.1 = 1</td>
<td>0</td>
</tr>
</tbody>
</table>
\[
\begin{array}{cc|cc|c}
1 & 0 & 0 & 1 & 1.1 = 1 \\
1 & 0 & 1 & 0 & 1.0 = 0 \\
1 & 1 & 0 & 1 & 1.1 = 1 \\
1 & 1 & 0 & 0 & 1.1 = 1 \\
\end{array}
\]

\[
\left\{ \begin{array}{c}
0 \\
1 \\
1 \\
0 \\
\end{array} \right\} Q_n
\]

\[T = J \overline{Q_n} + KQ_n = (J+Q_n)(K+\overline{Q_n})\]

08. Ans: 1.5
Sol:

<table>
<thead>
<tr>
<th>C/\text{k}</th>
<th>Q_1</th>
<th>Q_2</th>
<th>Q_3</th>
<th>Q_4</th>
<th>Q_5</th>
<th>Y = Q_3 + Q_5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The waveform at OR gate output, \(Y\) is \([A = +5V]\)

\[\begin{array}{c|c|c|c|c|c|c}
0 & T & 2T & 3T & 4T & 5T \\
\hline
T_1 = 5T
\end{array}\]

Average power

\[
P = \frac{V_{ao}^2}{R} = \frac{1}{R} \int_{T_1}^{t_1} \frac{1}{t_1} \int_{T_1}^{t_1} y^2(t) dt
\]

\[
= \frac{1}{RT_1} \left[ \int_{T}^{2T} A^2 dt + \int_{3T}^{5T} A^2 dt \right]
\]

\[
= \frac{A^2}{RT_1} \left[ (2T-T) + (5T-3T) \right]
\]

\[
= \frac{A^2}{RT_1} \cdot 3T = \frac{5\cdot 3}{10\times 5} = 1.5\text{mW}
\]

6. A/D and D/A Converters

01. Ans: (b)
Sol:

<table>
<thead>
<tr>
<th>CLK</th>
<th>Counter</th>
<th>Decoder</th>
<th>V_0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_2</td>
<td>Q_1 Q_0</td>
<td>D_3 D_2 D_1 D_0</td>
<td>V_0</td>
</tr>
<tr>
<td>1</td>
<td>0 0 0</td>
<td>0 0 0 0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0 0 1</td>
<td>0 0 0 1 0 1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0 1 0</td>
<td>0 0 1 0 2 0</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>0 1 1</td>
<td>0 0 1 0 2 0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>1 0 0</td>
<td>1 0 0 0 0 8</td>
<td>8</td>
</tr>
<tr>
<td>6</td>
<td>1 0 1</td>
<td>1 0 0 1 0 9</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>1 1 0</td>
<td>1 0 0 0 1 0</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>1 1 1</td>
<td>1 0 0 1 1 1</td>
<td>11</td>
</tr>
</tbody>
</table>

02. Ans: (b)
Sol:

\[R_{equ} = \frac{R}{10k} \Omega\]

\[I = \frac{V_R}{10k} = 1\text{mA.}\]

Current division at \(\frac{I}{16}\)
03. Ans: (c)
Sol: Net current at inverting terminal,
\[ I_i = \frac{1}{4} + \frac{1}{16} = \frac{5I}{16} \]
\[ V_0 = -I_i R = -\frac{5I}{16} \times 10k\Omega \]
\[ = -\frac{5 \times 1 \times 10^{-3} \times 10 \times 10^3}{16} = -3.125\text{V} \]

04. Ans: (d)
Sol: Given that \( V_{DAC} = \sum_{n=0}^{3} 2^{-n}b_n \) Volts
\[ V_{DAC} = 2^{-1}b_0 + 2^0b_1 + 2^1b_2 + 2^2b_3 \]
\[ \Rightarrow V_{DAC} = 0.5b_0 + b_1 + 2b_2 + 4b_3 \]
Initially counter is in 0000 state

<table>
<thead>
<tr>
<th>Up counter o/p</th>
<th>( V_{DAC}(V) )</th>
<th>o/p of comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>( b_3 b_2 b_1 b_0 )</td>
<td>( V_{DAC}(V) )</td>
<td>( \text{o/p of comparator} )</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>1.5</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>2.5</td>
<td>1</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>3.5</td>
<td>1</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>4.5</td>
<td>1</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>5.5</td>
<td>1</td>
</tr>
</tbody>
</table>

When \( V_{DAC} = 6.5 \text{V} \), the o/p of comparator is ‘0’. At this instant, the clock pulses to the counter are stopped and the counter remains in 1101 state.

\[ \therefore \text{The stable reading of the LED display is 13.} \]

05. Ans: (b)
Sol: The magnitude of error between \( V_{DAC} \) & \( V_{in} \) at steady state is \( |V_{DAC} - V_{in}| = |6.5 - 6.2| \)
\[ = 0.3 \text{V} \]

06. Ans: (a)
Sol: In Dual slope
\[ \text{ADC: } V_{in} T_1 = V_R T_2 \]
\[ \Rightarrow V_{in} = \frac{V_R T_2}{T_1} = \frac{100 \text{mV} \times 370.2 \text{ms}}{300 \text{ms}} \]
DVM indicates = 123.4

07. Ans: (d)
Sol: Ex: \( f_{in} = 1 \text{kHz} \rightarrow f_s = 2 \text{kHz} \)
\[ f_{in} = 25 \text{kHz} \leftarrow f_s = 50 \text{kHz} \]
1. Max conversion time = \( 2^{N+1}T = 2^{11.1} \mu\text{s} \)
\[ = 2048 \mu\text{s} \]
2. Sampling period = \( T_s \geq \text{maximum conversion time} \)
\[ T_s \geq 2048 \mu\text{s} \]
3. Sampling rate \( f_s = \frac{1}{T_s} \leq \frac{1}{2048 \times 10^{-6}} \)

\[ f_s \leq 488 \quad f_s \leq 500 \text{ Hz} \]

4. \( f_{in} = \frac{f_s}{2} = 250 \text{ Hz} \)

08. Ans: (d)

Sol: In an ADC along with S-H circuit (sample and hold) circuit, to avoid error at output, voltage across capacitor should not drop by more than \( \pm \Delta / 2 \), where \( \Delta \) is step size.

Here, \( \Delta = \frac{10 - 0}{(2^{10} - 1)} = 9.775 \times 10^{-3} \text{ V} \)

Hence \( \Delta / 2 = 4.8875 \times 10^{-3} \text{ V} \)

So conversion time (maximum) should be such that the drop across capacitor voltage must reach maximum value \( \Delta / 2 \).

Hence, time taken for this

\[ t = \frac{\Delta / 2}{\text{drop rate}} = \frac{4.8875 \times 10^{-3}}{10^{-3} \text{ V/msec}} \]

\[ t \approx 49 \text{ msec} \]

7. Architecture, Pin Details 8085 & Interfacing with 8085

01. Ans: (a)

Sol: chip select is an active low signal for \( \text{chipselect} = 0 \); the inputs for NAND gate must be let us see all possible cases for \( \text{chipselect} = 0 \) condition

\[
\begin{array}{cccccccccccc}
A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\
0 & 0 & 0 & 0 & 0 & 0 & X & X \\
0 & 0 & 1 & 1 & 0 & 0 & X & X \\
\end{array}
\]

:: Address space is 60H to 63H

\( A_0 \) to \( A_{11} \) are used for line selection

\( A_{12} \) to \( A_{15} \) are used for chip selection

\[
\begin{array}{cccccccccc}
A_{15} & A_{14} & A_{13} & A_{12} & A_{11} & \ldots & \ldots & \ldots & A_0 \\
1 & 1 & 1 & 0 & 0 & \ldots & \ldots & \ldots & 0 \\
\end{array}
\]

\( = \text{E000H} \)

\[
\begin{array}{cccccccccc}
1 & 1 & 1 & 0 & 1 & \ldots & \ldots & \ldots & 1 \\
\end{array}
\]

\( = \text{EFFFH} \)
02. Ans: (d)
Sol: • Both the chips have active high chip select inputs.
• Chip 1 is selected when \( A_8 = 1, A_9 = 0 \)
  Chip 2 is selected when \( A_8 = 0, A_9 = 1 \)
• Chips are not selected for combination of 00 & 11 of \( A_8 \) & \( A_9 \)
• Upon observing \( A_8 \) & \( A_9 \) of given address Ranges, F800 to F9FF is not represented

03. Ans: (d)
Sol: The I/O device is interfaced using “Memory Mapped I/O” technique.
The address of the Input device is
\[
\begin{array}{cccccccccccccccc}
A_{15} & A_{14} & A_{13} & A_{12} & A_9 & A_8 & A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\
1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 \\
\end{array}
\]
This mapping is memory mapped I/O

04. Ans: (b)
Sol: Out put 2 of 3×8 Decoder is used for selecting the output port. 
Select code is 010
\[
A_{15} \ A_{14} \ A_{13} \ A_{12} \ A_{11} \ A_{10} -- A_0
\]
\[
0 \ 1 \ 0 \ 1 \ 0 \ 0 \ --- \ - \ 0
\]
\[\Rightarrow 5000H\]

05. Ans: (d)
Sol: The Instruction for correct data transfer is
\[= LDA F8F8H\]

06. Ans: (a)
Sol: Address Range given is

\[
\begin{array}{cccccccccccccccc}
A_{15} & A_{14} & A_{13} & A_{12} & A_9 & A_8 & A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\
1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\
\end{array}
\]
To provide CS as low, the condition is
\[ A_{15} = A_{14} = 0 \text{ and } A_{13} A_{12} = 01 \text{ (or) } 10 \]
i.e. \[ A_{15} = A_{14} = 0 \text{ and } A_{13} A_{12} \text{ shouldn’t be } 00, 11. \]
Thus it is \[ A_{15} + A_{14} + [A_{13} A_{12} + \overline{A_{13}} \overline{A_{12}}] \]

**07. Ans:** (a)

**Sol:**

\[
\begin{array}{c}
A_{15} \\
A_{13} \\
A_{12} \\
A_{11} \\
3:8 \\
\text{Decoder}
\end{array}
\]

A_{15}, A_{14} are used for chip selection
A_{13}, A_{12}, A_{11} are used for input of decoder

<table>
<thead>
<tr>
<th>A_{15}</th>
<th>A_{14}</th>
<th>A_{13}</th>
<th>A_{12}</th>
<th>A_{11}</th>
<th>A_{10}</th>
<th>\ldots</th>
<th>A_0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Enable</td>
<td>Input</td>
<td>Address</td>
<td>of</td>
<td>decoder</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>of decoder</td>
<td>of chip</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Size of each memory block = \(2^{11} = 2K\)

**8. Instruction set of 8085 & Programming with 8085**

**01. Ans:** (c)

**Sol:**

6010H : LXI H, 8A79H ; (HL) = 8A79H
6013H : MOV A, L ; (A)←(L) = 79
6014H : ADD H ; (A) = 0111 1001
\[ + \]
\[ (H) = 1000 1010 \]

**02. Ans:** (c)

**Sol:**

6015H : DAA ; (A) = 0000 0011
\[ \text{CY} = 1, \text{AC} = 1 \]
6016H : MOV H, A ; (H)←(A) = 69H
6017H : PCHL ; (PC)←(HL) = 6979H

**03. Ans:** (c)

**Sol:**

SUB1 : MVI A, 00H  \(A\leftarrow 00H\)
CALL SUB2 \(\rightarrow\) program will shifted to SUB 2 address location

\[
\begin{array}{c}
\text{A} \\
\text{SUB 2 : INR A} \rightarrow 01H \\
\text{RET} \rightarrow \text{returned to the main program} \\
\end{array}
\]

\[
\begin{align*}
\text{: } & \text{The contents of Accumulator after execution of the above SUB2 is 02H.} \\
\end{align*}
\]

**04. Ans:** (c)

**Sol:**

The loop will be executed until the value in register equals to zero, then,

Execution time

\[
\begin{align*}
\text{SUB 1 : MVI A, 00H} & \text{ A} \leftarrow \text{00H} \\
\text{CALL SUB2} & \text{ \rightarrow program will shifted to SUB 2 address location} \\
\end{align*}
\]
\[ = 9(7T + 4T + 4T + 10T) + (7T + 4T + 4T + 7T) + 7T \]
\[ = 254T \]

### Question 05
**Ans: (d)**

**Sol:**
- \( H = 255 \) : \( L = 255, 254, 253, \ldots, 0 \)
- \( H = 254 \) : \( L = 0, 255, 254, \ldots, 0 \)
- \( H = 1 \) : \( L = 0, 255, 254, 253, \ldots, 0 \)
- \( H = 0 \) : 

  - In first iteration (with \( H = 255 \)), the value in \( L \) is decremented from 255 to 0 i.e., 255 times.
  - In further remaining 254 iterations, the value in \( L \) is decremented from 0 to 0 i.e., 256 times.

  \( \therefore \) ‘DCRL’ instruction gets executed for \( 256 \times 254 \times 65279 \) times.

### Question 06
**Ans: (a)**

**Sol:**
“STA 1234H” is a 3-Byte Instruction and it requires 4 Machine cycles (Opcode fetch, Operand1 Read, Operand2 Read, Memory write). The Higher order Address \((A_{15} - A_8)\) sent in 4 machine cycles is as follows:

- Given “STA 1234” is stored at 1FFEH i.e., Address Instruction
- 1FFE, 1FF, 2000 : STA 1234H

<table>
<thead>
<tr>
<th>Machine cycle</th>
<th>Address ((A_{15} - A_0))</th>
<th>Higher order address ((A_{15} - A_8))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Opcode fetch</td>
<td>1FFEH</td>
<td>1FH</td>
</tr>
</tbody>
</table>

### Question 07
**Ans: (d)**

**Sol:**
The operation SBI \( B_{H} \) indicates \( A - B \rightarrow A \) where \( A \) indicates accumulator.

Thus the result of the subtraction operation is stored in the accumulator and the contents of accumulator are changed.

### Question 08
**Ans: (c)**

**Sol:**
If the content in register B is to be multiplied with the content in register C, the contents of register B is added to the accumulator (initial value of accumulator is 0) for \( C \) times.