ACE
Engineering Academy
(Leading institute for ESE/GATE/PSUs)

ESE – 2019 MAINS
OFFLINE TEST SERIES

ELECTRONICS & TELECOMMUNICATION ENGINEERING (E&T)

TEST – 5
SOLUTIONS

All Queries related to **ESE – 2019 MAINS Test Series** Solutions are to be sent to the following email address
testseries@aceenggacademy.com | Contact Us : 040 – 48539866 / 040 – 40136222

01. (a)

Sol: Percentage regulation of transformer = (%R) $\cos\phi_2 \pm$ (%X) $\sin\phi_2$

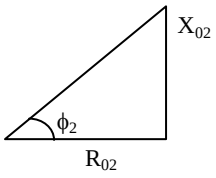
Max. regulation occurs at only lag pf load

Hence % regulation = (%R) $\cos\phi_2$ + (%X) $\sin\phi_2$

Condition for Maximum Regulation is $\frac{d(\%\,Reg)}{d\phi_2} = 0$

$$\phi_2 = \tan^{-1}\frac{(\%X)}{(\%R)}\ \text{lag}$$

$$= \tan^{-1}\left(\frac{X_{02}}{R_{02}}\right)\text{lag}$$



Impedance triangle at maximum regulation is show in figure

From the above, pf of load corresponding to maximum regulation = $\cos\phi_2 = \frac{\%R}{\%Z}; \sin\phi_2 = \frac{\%X}{\%Z}$

$\therefore$ Max. regulation = $(\%R)\left(\frac{\%R}{\%Z}\right)+(\%X)\left(\frac{\%X}{\%Z}\right)$

$$= \frac{(\%R)^2+(\%X)^2}{\%Z} = \%Z$$

01. (b)

Sol: Given,

Radius of rotor blade, r = 6m

Wind velocity, V = 16 ms^{-1}

Density of air, ρ = 1.24 kg $|m^3$

Wind turbine efficiency, η = 0.45[45%]

We know,

Electrical power out put of a wind turbine, $P_\circ = \frac{1}{2}\eta\rho AV^3$

$$P_\circ = \frac{1}{2}\eta\rho(\pi r^2)V^3$$

$$P_\circ = \frac{1}{2}\times 0.45\times 1.24\times\pi\times(6)^2\times 16^3$$

$$P_\circ = 129.24KW$$

$\therefore$ Electrical power out put = 129.24KW

01. (c)

Sol: <u>Channel Length Modulation:</u>

Channel Length Modulation (CLM) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance.

The effective channel length dependency on the drain to source voltage is named as Channel Length Modulation (CLM). It occurs when the width of the depletion layer is increased at the drain as drain voltage increases.

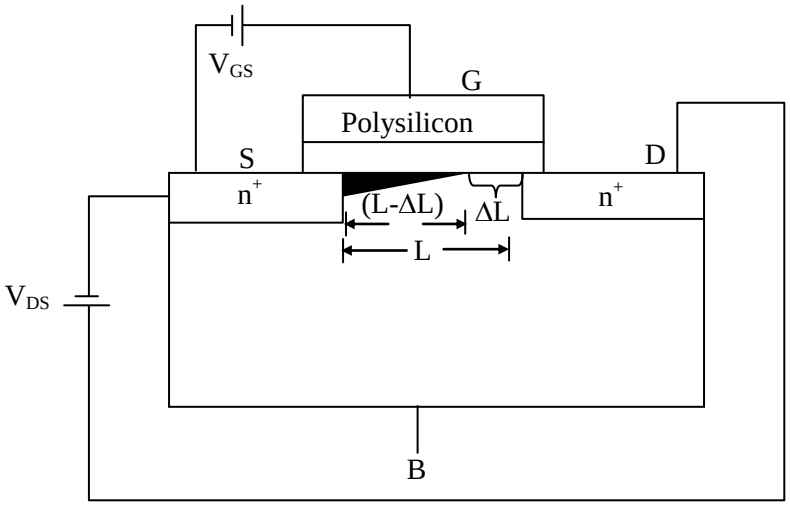


Fig. Channel Length Modulation

It is assumed that channel length remains constant as the drain voltage is increased appreciably beyond the on set of saturation. As a consequence, the drain current remains constant in the saturation region. In practice, however the channel length shortens as the drain voltage is increased. For long channel lengths, say more than 5μm, this variation of length is relatively very small compared to the total length and is of little consequence. However, as the device sizes are scaled down, the variation of length becomes more and more predominant and should be taken into consideration. As a consequence, the drain current increases with increase in drain voltage even in the saturation region.

A higher drain current is achieved by having a short effective channel length. Shorter effective channel length also caused higher mobility of electrons, which leads to a better performance especially for high-speed devices.

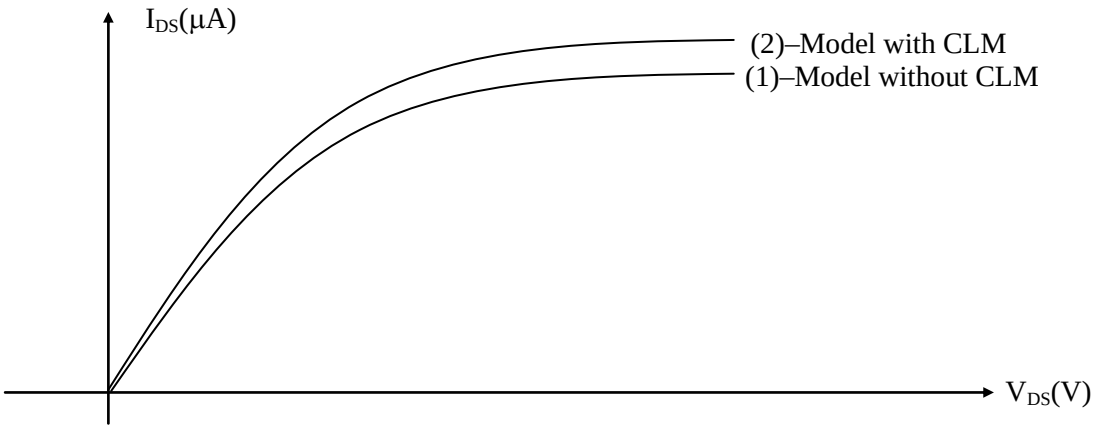
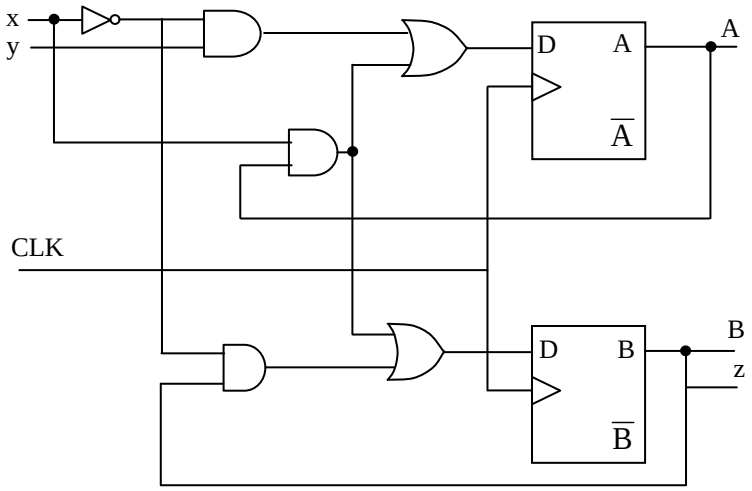


Figure. Comparison in current-voltage characteristics with and without CLM model

01. (d)

Sol:

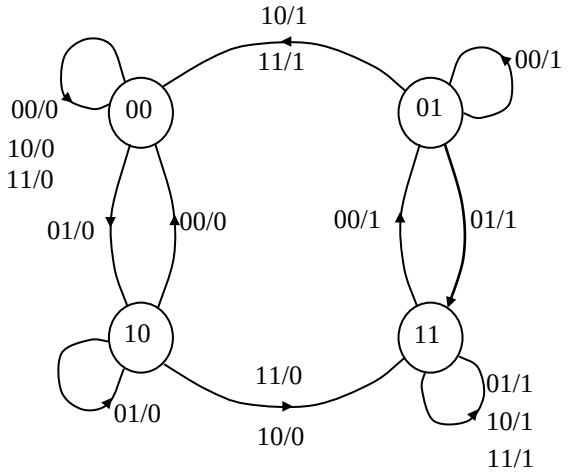
(i)



(ii)

Present state	Inputs	Next state	Output
A B	x y	A B	Z
0 0	0 0	0 0	0
0 0	0 1	1 0	0
0 0	1 0	0 0	0
0 0	1 1	0 0	0
0 1	0 0	0 1	1
0 1	0 1	1 1	1
0 1	1 0	0 0	0
0 1	1 1	0 0	0
1 0	0 0	0 0	0
1 0	0 1	1 0	0
1 0	1 0	1 1	1
1 0	1 1	1 1	1
1 1	0 0	0 1	1
1 1	0 1	1 1	1
1 1	1 0	1 1	1
1 1	1 1	1 1	1

(iii)

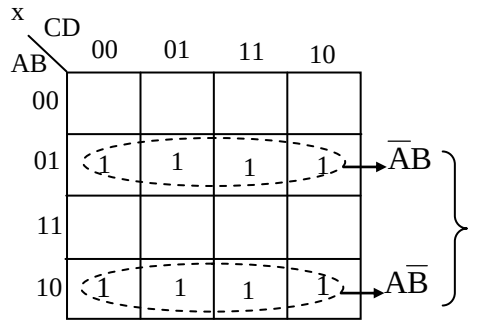


01. (e)

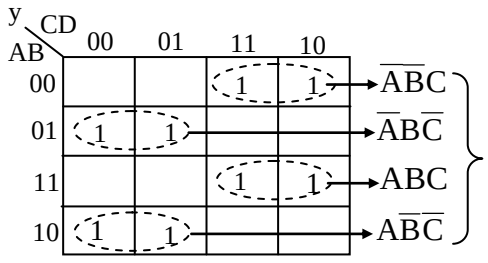
Sol:

A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

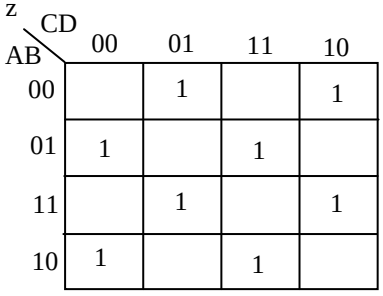
From truth table, we can observe that W = A



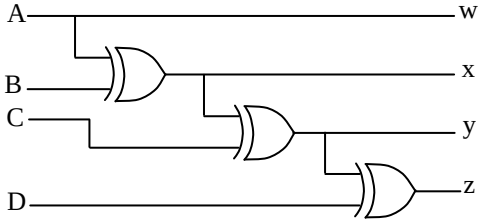
$$x = \overline{A}B + A\overline{B} = A \oplus B$$



$$y = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + ABC + A\overline{B}\,\overline{C}$$
$$y = \overline{A}\left(\overline{B}C + B\overline{C}\right) + A\left(BC + \overline{B}\,\overline{C}\right)$$
$$y = \overline{A}\left(B \oplus C\right) + A\overline{\left(B \oplus C\right)}$$
$$y = A \oplus B \oplus C$$
$$y = x \oplus C$$



$$z = A \oplus B \oplus C \oplus D$$
$$z = y \oplus D$$



02. (a)

Sol: From short-circuit data,

$r_{eH} = \frac{P_{sc}}{I_{sc}^2} = \frac{100}{(4)^2} = 6.25\Omega$

and $Z_{eH} = \frac{V_{sc}}{I_{sc}} = \frac{60}{4} = 15\Omega$

then, $X_{eH} = \sqrt{Z_{eH}^2 - r_{eH}^2} = 13.61\Omega$

For the LV side, the parameters are given as,

$r_{eL} = 6.25\left(\frac{1}{5}\right)^2 = 0.25\Omega$

$X_{eL} = 13.61\left(\frac{1}{5}\right)^2 = 0.544\Omega$

Now, Full load secondary current is,

$I_{2L} = \frac{10000}{400} = 25\,A$

Therefore, $E_2 - V_2 = I_{2L}\, r_{eL} \cos\theta_2 + I_{2L}\, X_{eL} \sin\theta_2$

$\Rightarrow E_2 - 400 = (25)\,(0.25)\,(0.8) + (25)\,(0.544)\,(0.6)$

$\Rightarrow E_2 = 413.16$ V

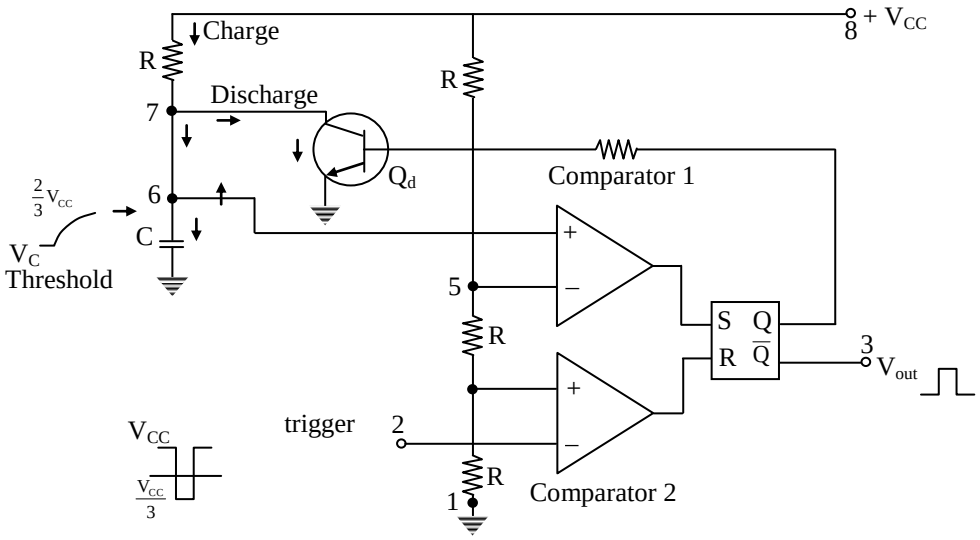
Then the voltage applied at the primary (HV) side is ,

$= 413.16 \times \frac{2000}{400} = 2065.8\,V$

02. (b)

Sol: **<u>Monostable multivibrator using 555 timer:</u>**

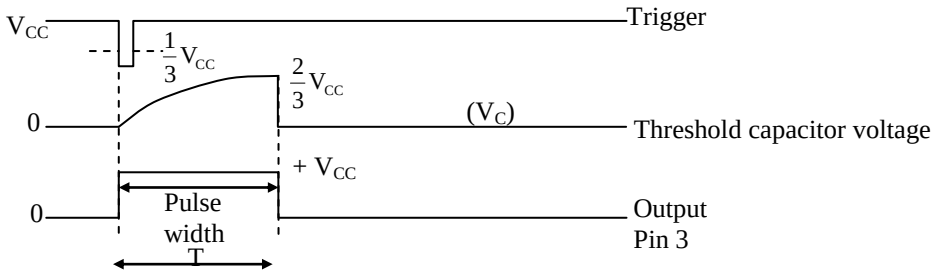
(i) A monostable multivibrator often called a one-shot multivibrator, is a pulse generator circuit in which the duration of the pulse is determined by the R-C network, connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable). For auto-triggering of output from quasi-stable state to stable state energy is stored by an externally connected capacitor C to a reference level. The time taken in storage determines the pulse width. The transition of output from stable state to quasi-stable state is accomplished by external triggering. The functional block of monostable mode of operation is shown in figure.



Operation

Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor - C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below +1/3 V_{cc}, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cut-off, the capacitor C begins charging toward + V_{cc} through resistance R with a time constant equal to RC. When the increasing capacitor voltage becomes slightly greater than +2/3 V_{CC}, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low. Thus the output returns back to stable state from quasi-stable state.

The output of the monostable multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats. Trigger input, output voltage and capacitor voltage waveforms are shown in figure.



(ii) Derivation for pulse width

The voltage across capacitor increases exponentially and is given by

$V_C = V(1 - e^{-t/CR})$

At t = T, $V_C = 2/3\ V_{CC}$

then $$\frac{2}{3}V_{CC} = V_{CC}\left(1 - e^{-T/CR}\right)$$

$$\frac{2}{3} - 1 = -e^{-T/CR}$$

$$\frac{1}{3} = e^{-T/CR}$$

$$-\frac{T}{CR} = -1.0986$$

$$T = +\ 1.0986\ CR$$

$$T = 1.1\ CR$$

Where C in farads, R in ohms, T in seconds.

Key points : Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e 1.1 RC.

Thus the pulse width denoted as W is given by.

W = 1.1 R.C.

02. (c)

Sol:

(i) $F_1 = \bar{x}\,\bar{y}\,\bar{z} + xz = \bar{x}\,\bar{y}\,\bar{z} + xz(y + \bar{y})$

$= \bar{x}\,\bar{y}\,\bar{z} + x\bar{y}z + xyz$

$F_1 = \Sigma m(0,5,7)$

$F_2 = x\bar{y} + \bar{x}y = x\bar{y}\,\bar{z} + \bar{x}y(\bar{z} + z)$

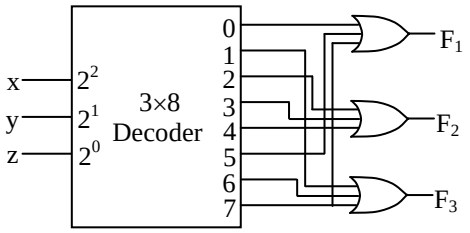
$= x\bar{y}\,\bar{z} + \bar{x}y\bar{z} + \bar{x}yz$

$F_2 = \Sigma m(2,3,4)$

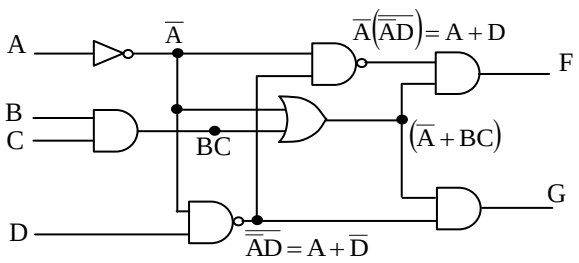
$F_3 = \bar{x}\,\bar{y}z + xy = \bar{x}\,\bar{y}z + xy(\bar{z} + z)$

$= \bar{x}\,\bar{y}z + xy\bar{z} + xyz$

$F_3 = \Sigma m(1,6,7)$

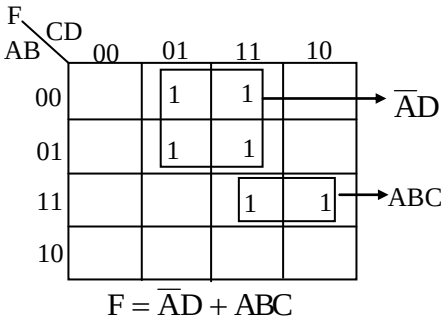


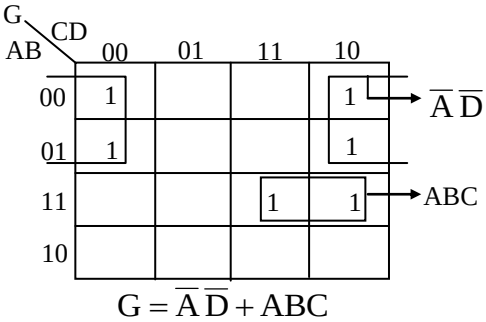
(ii)



$F = (A + D)(\bar{A} + BC) = ABC + \bar{A}D + BCD$

$G = (A + \bar{D})(\bar{A} + BC) = ABC + \bar{A}\,\bar{D} + BC\bar{D}$





03. (a)

Sol: Given, 25 hp , 230 V, 50 Hz,
60 A, at 0.866 lag
P_{cu} = 850 W ; P_{core} = 450 W
P_{cu} r = 1050 W; P_{ro} t = 500 W

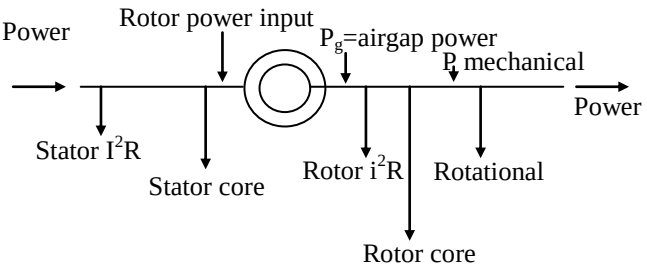


Fig. Power flow diagram

$P_{input} = \sqrt{3}VI\cos\theta = \sqrt{3} \times 230 \times 60 \times 0.866$
$= 20699.39$ W

(i) Rotor Power input = Airgap power (P_g)

$P_g = P_{input}$ – stator I_r^2 losses – stator core loss

$P_g = 20699.39 – 850 – 450$

$= 19399.392$ W

(ii) In an induction motor rotor ohmic losses = SP_{ag}

Given rotor ohmic losses,

$\Rightarrow \quad 1050 = S \times 19399.392$

$$\text{Slip, } S = \frac{1050}{19399.392} = 0.054125$$

$$\simeq 0.054$$

(iii) Mechanical power developed

$= P_g – P_{\text{rotor ohmic losses}}$

$= 19399.392 – 1050 = 18349.392$

Also mechanical power developed

$= (1 – s)P_{ag} = (1 – 0.054125)19399.39$

$= 18749.392$

(iv) Output power = $P_{mech} – P_{rotational}$

$= 18349.392 – 500$

$P_{out} = 17849.392$

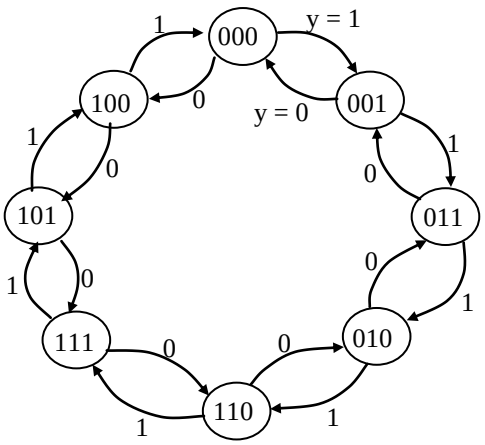
(v) Now $\%\eta = \frac{P_{out}}{P_{in}}$

$$= \frac{17849.392}{20695.39} \times 100$$

$= 86.231\%$

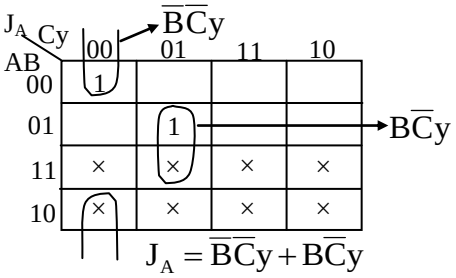
03. (b)

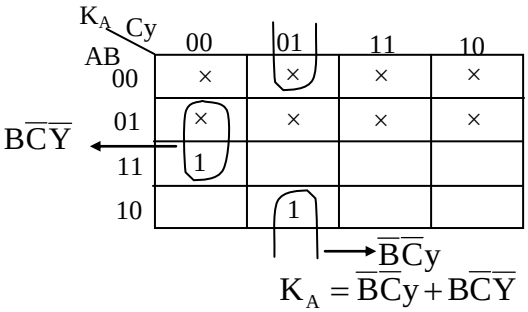
Sol: The state diagram is

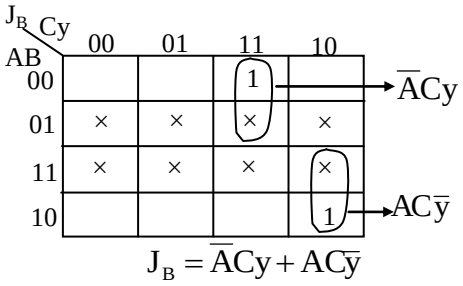


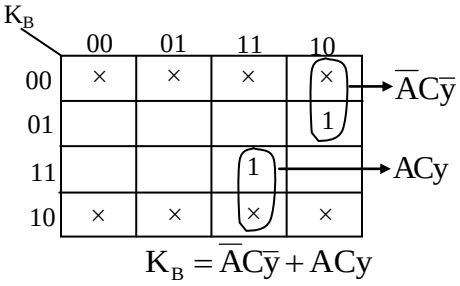
State table:

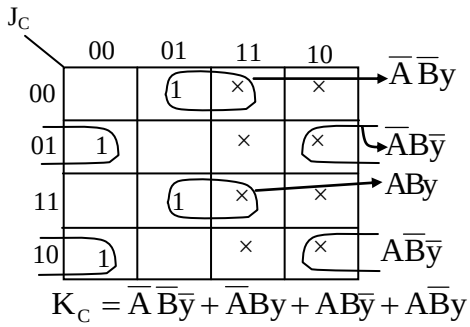
Present state A B C y	Next state A B C	Flip-flop inputs		
		J_A K_A	J_B K_B	J_C K_C
0 0 0 0	1 0 0	1 ×	0 ×	0 ×
0 0 0 1	0 0 1	0 ×	0 ×	1 ×
0 0 1 0	0 0 0	0 ×	0 ×	× 1
0 0 1 1	0 1 1	0 ×	1 ×	× 0
0 1 0 0	0 1 1	0 ×	× 0	1 ×
0 1 0 1	1 1 0	1 ×	× 0	0 ×
0 1 1 0	0 0 1	0 ×	× 1	× 0
0 1 1 1	0 1 0	0 ×	× 0	× 1
1 0 0 0	1 0 1	× 0	0 ×	1 ×
1 0 0 1	0 0 0	× 1	0 ×	0 ×
1 0 1 0	1 1 1	× 0	1 ×	× 0
1 0 1 1	1 0 0	× 0	0 ×	× 1
1 1 0 0	0 1 0	× 1	× 0	0 ×
1 1 0 1	1 1 1	× 0	× 0	1 ×
1 1 1 0	1 1 0	× 0	× 0	× 1
1 1 1 1	1 0 1	× 0	× 1	× 0

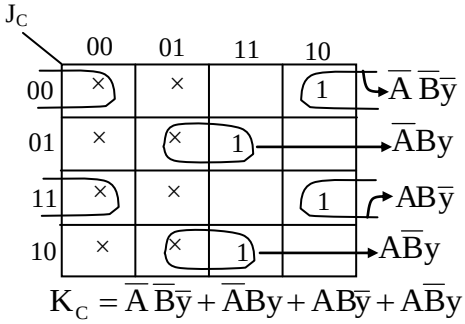


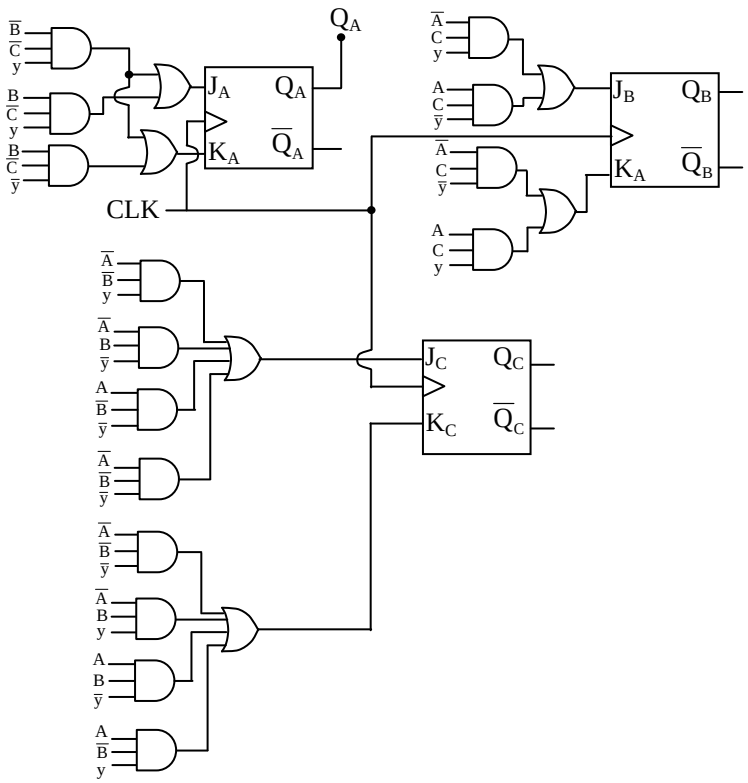












03. (c)

Sol: $$\beta(f)=\frac{V_o}{V_{in}}=\frac{\dfrac{R\left(\dfrac{1}{j\omega c}\right)}{R+\left(\dfrac{1}{j\omega c}\right)}}{R+\dfrac{1}{j\omega c}+\dfrac{R\left(\dfrac{1}{j\omega c}\right)}{R+\left(\dfrac{1}{j\omega c}\right)}}$$

$$\beta(f)=\frac{R\left(\dfrac{1}{j\omega c}\right)}{R^2+\dfrac{2R}{j\omega c}-\dfrac{1}{\omega^2c^2}}$$

$$=\frac{R}{3R+j\left(\omega R^2C-\dfrac{1}{\omega c}\right)}$$

According to Barkhausen criteria, condition to start the oscillations is that the magnitude of the loop gain ($A_v\beta$) must be unity. i.e $A_v.\beta = 1$.

$$R(3-A_v)+j\left(\omega R^2C-\frac{1}{\omega c}\right)=0$$

$R(3 - A_v) = 0$

$\Rightarrow A_{v.min} = 3.$

$\therefore$ Gain $(A_v) = 3.$

In RC phase-shift oscillator, cascaded RC networks determine the frequency.

$$\left(\omega R^2C-\frac{1}{\omega c}\right)=0.$$

$$\Rightarrow \omega=\frac{1}{RC}$$

$$\therefore \text{ Frequency of oscillation } (\omega)=\frac{1}{RC}.\text{rad/sec.}$$

$$\text{Frequency of oscillation } (f)=\frac{1}{2\pi RC}\text{Hz}$$

04. (a)

Sol: 240 V, series motor, I_a = 40 A at rated output, N = 1500 rpm

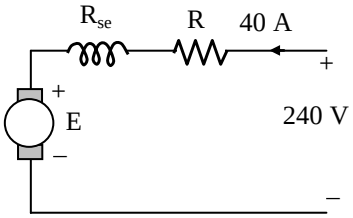
(i) Resistance to added to maintain rated torque At starting:

To maintain rated torque I_a should be rated current in I_a = 40A

Since $T \propto \phi I_a$ $\quad T \propto I_a^2 (\text{if } \phi \propto I_a)$

At starting speed of motor = 0,

$\Rightarrow N = 0 \Rightarrow$ EMF induced = 0



E = 0 ; $V = I_a (r_a + R)$

$240 = 40 (0.3 + R)$

$R = 5.7\ \Omega$

$\therefore$ 5.7 Ω resistance should be added to maintain rated torque at starting.

(ii) Resistance to added to maintain rated torque at 1,000 rpm:

At 1500 rpm, $E = V – IR_{se}$

$E = 240 – 40 (0.3)$

$= 228$ V

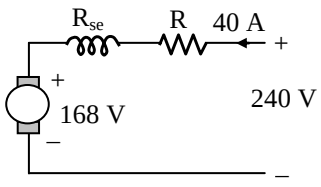
To maintain rated torque at 1000 rpm,

I_a = 40 A i.e., rated current

Since $E \propto \phi N$ and $\phi \propto I_a$

I_a remains constant

$E \propto N$



$\therefore \frac{228}{E} = \frac{1500}{1000} \Rightarrow E = 152\ V$

$240 = 152 + 40\ (0.3 + R)$

$R = 1.9\Omega$

$\therefore$ Resistance to be inserted = 1.9 Ω.

04. (b)

Sol: kW demand of Load:

$= 250W + 100kw = 350kW$

kVAR demand of Load

$= \frac{250k}{0.95} \times \sin[\cos^{-1} 0.95] + \frac{100k}{0.8} \times \sin[\cos^{-1} 0.8]$

= 82.17 (Lag) + 75(Lead)

= 7.17 (Lag kVAR) [consuming]

kW supplied by Machine1 = 200kW.

kW supplied by Machine2

= Demand – 200kw = 150kW

K VAR supplied by Machine 1

$= \frac{200k}{0.9} \times \sin[\cos^{-1} 0.9]$

= 96.86 (delivered) [Lag]

Hence the other alternator must consume the reactive power by operating at Leading power factor and deliver the active power.

$\therefore$ kVAR consumed by machine 2

= 96.86-7.17 = 89.69kVAR

$\tan \phi = \frac{VI\sin\phi}{VI\cos\phi}$

$= \frac{89.69kVAR}{150kW} = 0.5979.$

$\phi = 30.87, \cos \phi = 0.858$ Lead

Hence near by Answer is $\underline{\sim}$ 0.89 Lead.

04. (c)

Sol: From the above figure,

$V_s = 60\sqrt{2} \sin \omega t$

$V_L = 24\ V$

The conduction begins at an angle of

$\alpha_1 = \sin^{-1}(V_L / V_m)$

$= \sin^{-1}(24 / 60\sqrt{2}) = 0.282 rad$

or 16.43^o

$\therefore \alpha = 16.43^o$

Conduction ceases at an angle of

$(\pi - 0.282)$ rad

Given $I_{peak} = 2.5A$

$I_{peak} = \frac{60\sqrt{2} - 24}{Rs} = 2.5$

$\therefore R_s = 24.34\ \Omega$

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} id(\omega t)$$

$$= \frac{1}{2\pi}\int_{\alpha}^{\pi-\alpha}\left[\frac{V_m \sin\omega t}{R_s} - V_L\right]d(\omega t)$$

$$= \frac{V_m}{\pi R_s}\cos\alpha - \frac{(\pi - 2\times\alpha_{1_{radian}})}{2\pi}\times\frac{V_L}{R_s}$$

$\alpha = 16.43^o$ or 0.282 radian

$R_s = 24.3\Omega$

$\therefore I_{dc} = 0.66$ A

$\therefore$ Time to deliver 20 Ah = $\frac{20}{0.66} \approx 30$hours

04. (d)

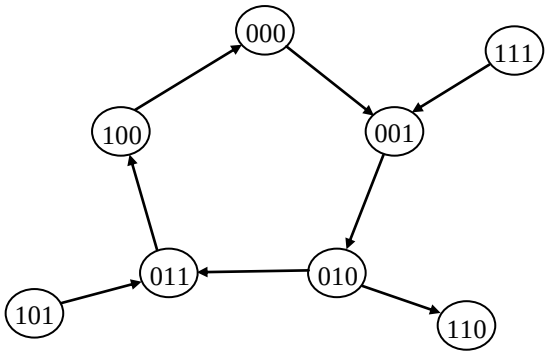
Sol: A self starting (or) correcting counter is one in which normally unused states will return to normal count sequence. If any of these unused states cannot return to the normal sequence the counter is said to be not self-correcting.

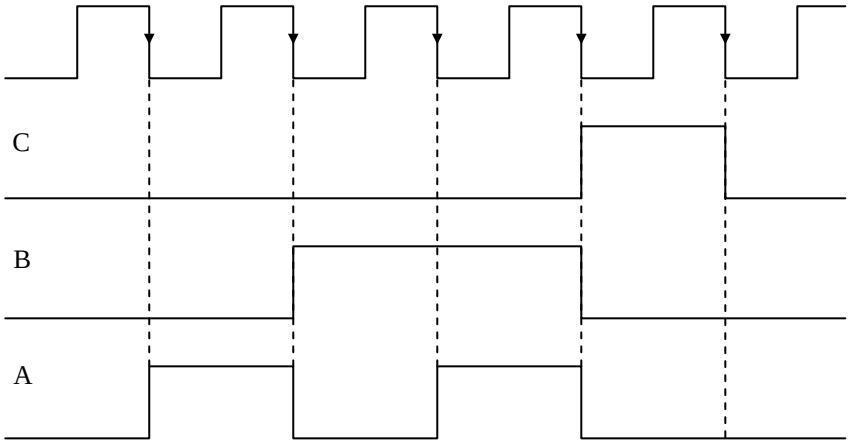
Present state	Control inputs			Next state
C B A	J_C K_C	J_B K_B	J_A K_A	C B A
0 0 0	0 0	0 0	1 1	0 0 1
0 0 1	0 0	1 1	1 1	0 1 0
0 1 0	0 0	0 0	1 1	0 1 1
0 1 1	1 0	1 1	1 1	1 0 0
1 0 0	0 1	0 0	0 0	0 0 0
1 0 1	0 1	1 1	0 0	0 1 1
1 1 0	0 1	0 0	0 0	0 1 0
1 1 1	1 1	1 1	0 0	0 0 1

$J_C = AB$, $K_C = C$, $J_B = A$, $K_B = A$; $J_A = K_A = \overline{C}$

Unused states are 101, 110, 111. This counter is a self starting counter, because state 101 goes to state 011 which is used state state 110 goes to 010 and state 111 goes to state 001. So, the modulus of the given counter is 5 and counting sequence is 000,001,010,011,100,000.

The state diagram and timing diagram are shown below.





SECTION-B

05. (a)

Sol: Given data, 1ϕ transformer

$N_1 = 500$ turns, $N_2 = 1000$ turns

$a = 12\ cm^2$, $l = 50$ cm and $\mu = 20000$

$$L_{11} = \frac{\mu N_1^2 a}{\ell}$$

$$= \frac{20000 \times 4\pi \times 10^{-7} \times 500 \times 500 \times 12 \times 10^{-4}}{5 \times 10^{-2}}$$

$= 15.07$ Henry

L_{12} = Inductance in coil 2 due to current in coil-1 = $\frac{N_2 \phi_1}{i_1}$

Since flux in transformer is constant, $\phi_1 = \phi$ = main flux

$$L_{12} = \frac{N_2 \phi}{i_1}$$

Also $L_{11} = \frac{N_1 \phi}{i_1} \Rightarrow \phi = \frac{L_{11} i_1}{N_1}$

By substitute ϕ in L_{12}

$$\therefore\ L_{12} = \frac{N_2}{i_1} \frac{L_{11} i_1}{N_1} = L_{11} \frac{N_2}{N_1} = 15.07 \times \frac{1000}{500}$$

$L_{12} = 30.159$ H

05. (b)

Sol: Condition for zero voltage Regulation:

Zero voltage regulation is possible only in leading power factors

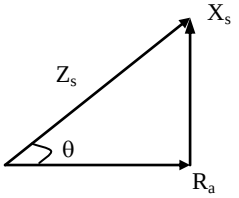
$E^2 = (V\cos\phi + I_aR_a)^2 + (V\sin\phi - I_aX_s)^2$

$= V^2\cos^2\phi + I_a^2R_a^2 + 2VI_aR_a\cos\phi + V^2\sin^2\phi + I_a^2X_s^2 - 2VI_aX_s\sin\phi$

$E^2 = V^2 + I_a^2z_s^2 + 2VI_a[R_a\cos\phi - X_s\sin\phi]$

$Z_s = R_a + jX_s = \sqrt{R_a^2 + X_s^2}$

Impedance angle (or) internal angle



$\theta = \tan^{-1}\left(\frac{X_s}{R_a}\right)$

$\theta \cong 90°$ ($\because R_a << X_s$)

$R_a = Z_s\cos\theta$ and $X_s = Z_s\sin\theta$

Generally θ range is 80° – 85°.

$E^2 = V^2 + I_a^2Z_s^2 + 2VI_a[Z_s\cos\theta\cos\phi - Z_s\sin\theta\sin\phi]$

$= V^2 + I_a^2Z_s^2 + 2VI_a.Z_s\cos(\theta+\phi)$

$= V^2 + I_aZ_s[I_aZ_s + 2V\cos(\theta+\phi)]$

$E^2 - V^2 = I_aZ_s[I_aZ_s + 2V\cos(\theta+\phi)]$

For zero regulation, $E^2 - V^2 = 0$ ($\because E = V$)

$I_aZ_s + 2V\cos(\theta+\phi) = 0$

Condition for zero regulation is

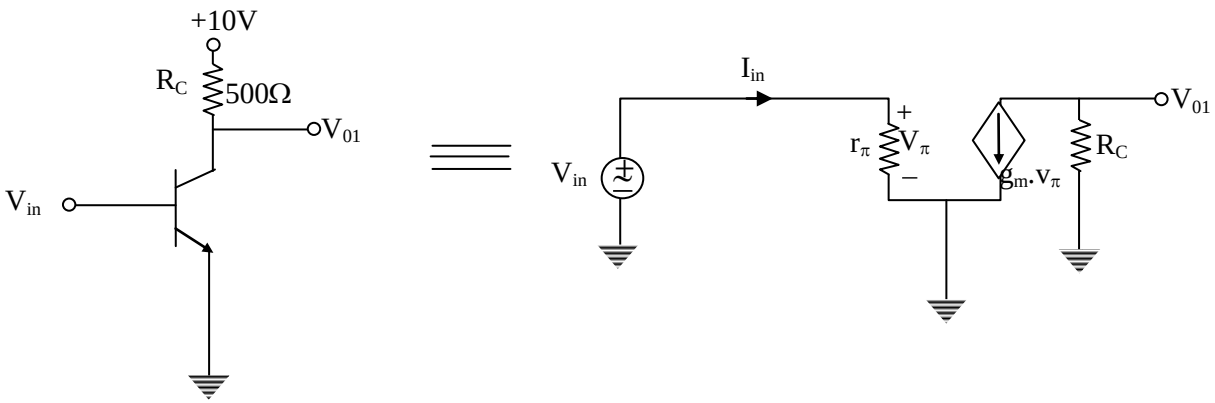
$\therefore \cos(\theta + \phi) = \frac{-I_aZ_s}{2V}$

05. (c)

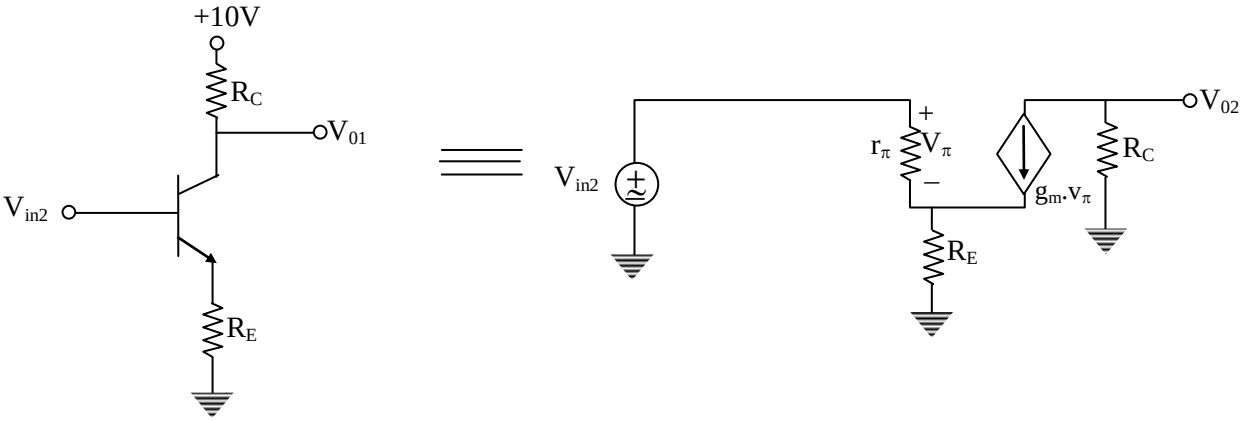
Sol:

(i) For CE configuration given in the figures, input impedances calculated for with and without emitter resistance as:

By small-signal analysis of the above circuits,



Input impedance $\left(R_{in_1}\right) = R_1 = r_\pi = 2.5k\Omega$



Input impedance $\left(R_{in_2}\right) = R_2 = [r_\pi + (1+ \beta)\, R_E]$

$$R_2 \cong r_\pi + \beta R_E \qquad (\because \beta >> 1)$$

$$= 2.5k\Omega + (100)\,(25\Omega)$$

$$\therefore \; R_2 = 5k\Omega$$

(ii) Voltage gain,

$$A_{V_1} = -g_m.R_C \quad \text{(without emitter resistance, } R_E\text{)}$$

$$A_{V_2} = -\frac{g_m.R_C}{\left(1+\left(\frac{1}{r_\pi}+g_m\right).R_E\right)} \quad \text{(with } R_E\text{)}$$

$$\frac{A_{V_1}}{A_{V_2}} = 1+\left(\frac{1}{r_\pi}+g_m\right).R_E$$

$$= 1+\left(\frac{g_m}{\beta}+g_m\right).R_E \qquad (\because \beta = g_m \,.\, r_\pi)$$

$$= 1+g_m\left(\frac{1}{\beta}+1\right)R_E$$

So, $\frac{A_{V_1}}{A_{V_2}} \approx 1+g_m.R_E = 1+\frac{\beta}{r_\pi}.R_E \qquad (\because \beta >> 1)$

$$= 1+\frac{100}{2.5k\Omega}\times 25\Omega$$

$$= 2$$

05. (d)

Sol: In a multi-stage amplifier, it is convenient to analyse the last stage (output stage) first.

In the present case, the last stage (Q_2 - stage) is emitter follower which has voltage gain of unity. Then the over all gain of two-stage amplifier (product of gains of individual stages) is same as gain of first stage which is common emitter amplifier in fig.

The gain of CE amplifier is

$$A_v = A_{v1} = \frac{r_{c1}}{r_{E1} + r_e'}$$

Since $R_E = 0$ (for Q_1 transistor), $r_{E1} = 0$

Then,

$$A_v = \frac{r_{c1}}{r_e'}$$

Where r_{c1} is the effective impedance seen by the collector of transistor Q_1.

That is,

$$r_{c1} = R_{C1} \,||\, Z_{i(base)2}$$

The impedance, $Z_{i(base)2}$ at the base of transistor Q_2 is,

$Z_{i(base)2} = \beta.R_{E2}$

$= 80 \times 3k$

or $Z_{i(base)2} = 240k\Omega$

Therefore,

$$R_{c1} = R_{C1} \,||\, Z_{i(base)2}$$

$$= 10k \,||\, 240k$$

or $r_{c1} = 9.6\ k\Omega$

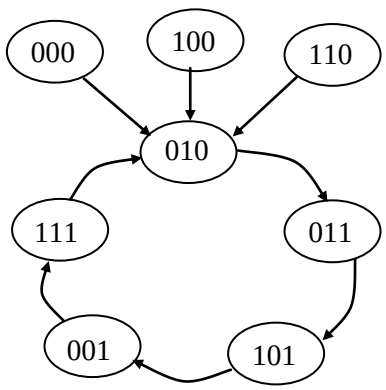
therefore, over all gain of amplifier of fig is

$$A_v = \frac{r_{c1}}{r_e'} = \frac{9.6 \times 10^3}{25} = 384$$

Or $A_v = 384$

05. (e)

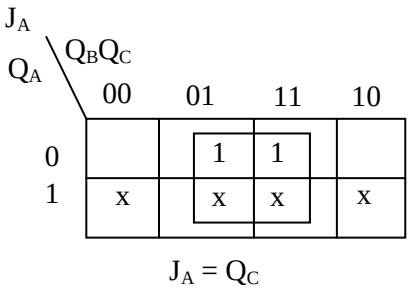
Sol: The state transition diagram for the counter is shown below



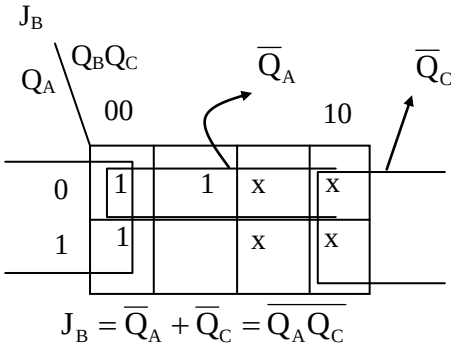
Counter excitation table shown below

Present State	Next State	Present input		
Q_A Q_B Q_C	Q_A Q_B Q_C	J_A K_A	J_B K_B	J_C K_C
0 0 0	0 1 0	0 X	1 X	0 X
0 0 1	1 1 1	1 X	1 X	X 0
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 1	1 X	X 1	X 0
1 0 0	0 1 0	X 1	1 X	0 X
1 0 1	0 0 1	X 1	0 X	X 0
1 1 0	0 1 0	X 1	X 0	0 X
1 1 1	0 1 0	X 1	X 0	X 1

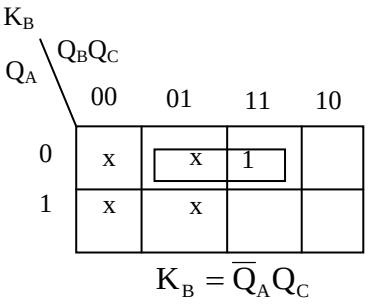
By observing the truth table $K_A = 1$



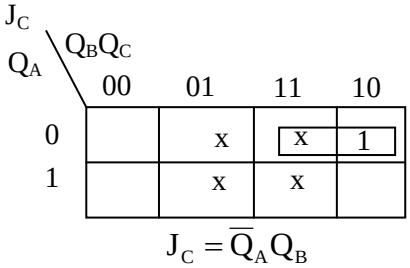
$J_A = Q_C$



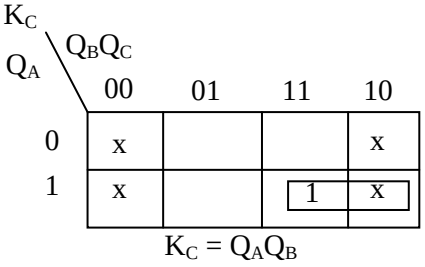
$J_B = \overline{Q}_A + \overline{Q}_C = \overline{Q_A Q_C}$



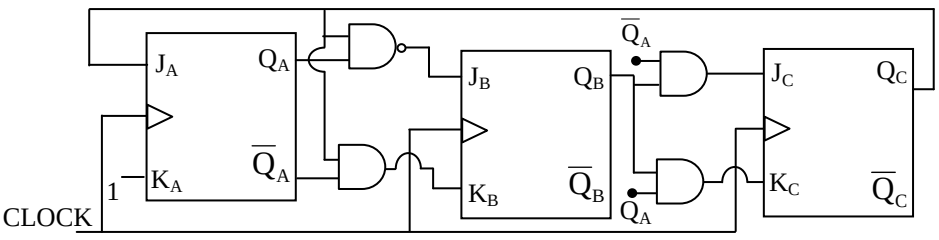
$K_B = \overline{Q}_A Q_C$



$J_C = \overline{Q}_A Q_B$



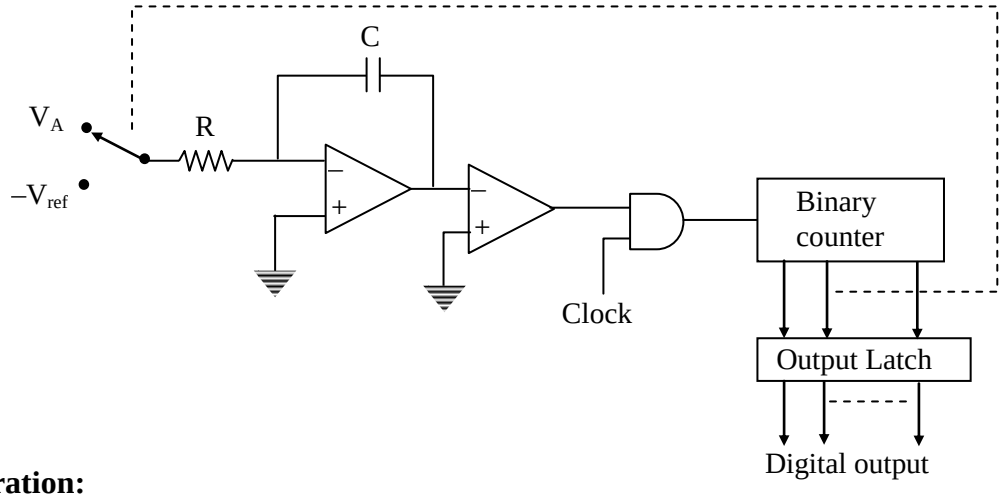
$K_C = Q_A Q_B$



05. (f)

Sol: In dual slope type ADC, the integrator generates two different ramps, one with the unknown analog input voltage V_A and another with a known reference voltage (V_{ref}).

The key advantage of this architecture over the single slope is that the final conversion result is insensitive to errors in the component values. That is, any error introduced by a component value during the integrate cycle will be cancelled out during the dc-integrate phase.



Operation:

The binary counter is initially reset. The output of integrator reset to 0V and the input to the ramp generator or integrator is switched to the unknown analog input voltage V_A.

The analog input voltage V_A is integrated by the inverting integrator and generates a negative ramp output. The output of comparator is positive and the clock is passed through AND gate. This results in counting up of the binary counter. The negative ramp continues for a fixed amount of time period t_1, which is determined by a count detector for the same period t_1. At the end of the fixed time period t_1, the ramp output of integration is given by,

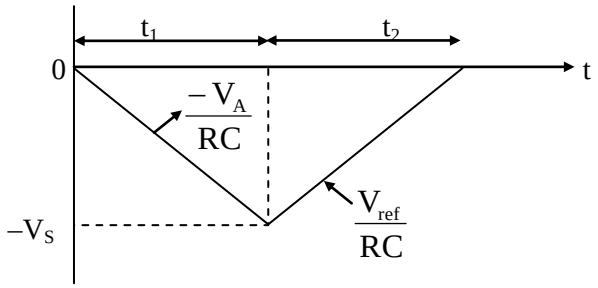
$$V_S = \frac{-V_A}{RC} \times t_1$$

When counter reaches a fixed count at the time period t_1. The binary counter resets to 0000 and switches the integrator input to a negative reference voltage $-V_{ref}$.

Now the ramp generator starts with the initial value $-V_S$ and increases in positive direction until it reaches 0V and counter gets advanced. When V_S reaches 0V, comparator output becomes negative (i.e., logic 0) and the AND gate is deactivated. Hence no further clock is applied through AND gate. Now the conversion cycle is said to be completed and the positive ramp voltage is given by,

$$V_S = \frac{V_{ref}}{RC} \times t_2$$

Where V_{ref} and RC are constants and time period t_2 is variable. The dual ramp output waveform is shown below.



Since ramp generator voltage starts at 0V, decreasing down to $-V_S$ and then increasing upto 0V. The amplitude of negative and positive ramp voltages can be equated as follows

$$\frac{V_{ref}}{RC} \times t_2 = \frac{-V_A}{RC} \times t_1 \Rightarrow V_A = \frac{-V_{ref}}{t_1} \times t_2$$

06. (a)

Sol: Given data

$P_0 = 10Hp$

$I_{fl} = 37.5A$

$V = 230V$

$\phi = 0.01Wb$

$P = 4$

$Z = 666$

$A = 2$

$R_a = 0.267\Omega$

Rotational losses = 600W

At, $N_1 = 1000$ rpm

Output torque = T_{sh} = ?

$$E_b = \frac{\phi ZN}{60}\frac{P}{A}$$

$$= \frac{0.01\times 666\times 1000}{60}\times\frac{4}{2}$$

$E_b = 222V$

$$I_a = \frac{V - E_b}{R_a} = \frac{230 - 222}{0.207}$$

$= 29.96A$

Gross mechanical power developed = P_{gm}

$P_{gm} = E_bI_a = 222 \times 29.96 = 6651.12W$

Output power = shaft power

$P_{sh} = P_{gm}$ – rotational losses

$P_{sh} = 6651.12 - 600$

$= 6051.12W$

$P_{sh} = T_{sh} \times \omega$

$$6051.12 = T_{sh} \times \frac{2\pi\times 1000}{60}$$

Output torque = $T_{sh} = 57.78N\text{-}m$

06. (b)

Sol: Performance parameters of logic families are,

(i) Fan-out and Fan-in

(ii) Input/output voltage levels

(iii) Noise margin

(iv) Rise and fall time and propagation delay

(v) power dissipation.

(i) Fan-in and Fan-out:-

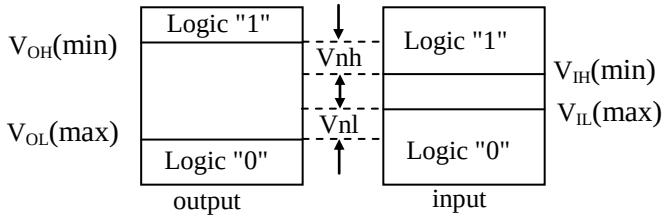
Fan - in is the maximum number of inputs a logic family can handle. Fan-in is not an electrical property and is a function of the manufacturing process.

A measure of the ability of the output of one gate to drive the inputs of subsequent gates is nothing but "fan-out". Typical fan-out for most TTL sub families is 10. Fan-out depends on the amount of electric current a gate can source or sink while driving other gates. The effects of loading a logic gate output with more than its rated fan-out will degrade the performance of the circuit.

The gate delay increases with increase in fan-out.

(ii) Input/output voltage levels:

There is a limit on voltage until it is considered HIGH. As we draw more and more current out of the HIGH level output, the output voltage drops lower and lower, until finally it will not be recognized as a HIGH level any more by the other TTL gates that it is feeding.



$V_{OH(min)}$: The minimum output voltage in HIGH state
$V_{OL(max)}$: The maximum output voltage in low state
$V_{IL(min)}$: The minimum input voltage guaranted to be recognized as logic"1"
$V_{IL(max)}$: The maximum input voltage guaranted to be recognized as logic "0"

$V_{OH} > V_{IH} > V_{IL} > V_{OL}$

(iii) Noise margin:-

Noise margin measures how much external electrical noise a gate can withstand before producing an incorrect output. TTL will take anything below about 0.8 volt as a 0, anything above about 2 volts as a high.

Low noise margin: [LNM]
The largest noise amplitude that is guaranteed not to change the output voltage level when superimposed on the input voltage of the logic gate (when this voltage is in the LOW).
$LNM = V_{IL(max)} - V_{OL(max)}$

High noise margin: [HNM]
The largest noise amplitude that is guaranteed not to change the output voltage level when superimposed on the input voltage of the logic gate (when this voltage is in the HIGH).
$HNM = V_{OH(min)} - V_{IH(min)}$
Noise margin = min(LNM, HNM).

(iv) Rise time, fall time and propagation delay:

Rise time (t_r) is the time, taken by the pulse to rise from 10% to 90% final voltage level.
Fall time (t_f) is the time taken by the pulse to fall from 10% to 90% of final voltage level.
Propagation delay is defined as the average of low to high(t_{PLH})
Propagation delay and high-to-low (t_{PHL}) propagation delay.

Propagation delay time, $t_p = \frac{(t_{PHL}) + (t_{PHL})}{2}$

Propagation delay is directly proportional to the switching time and increases as the fan-out increases.

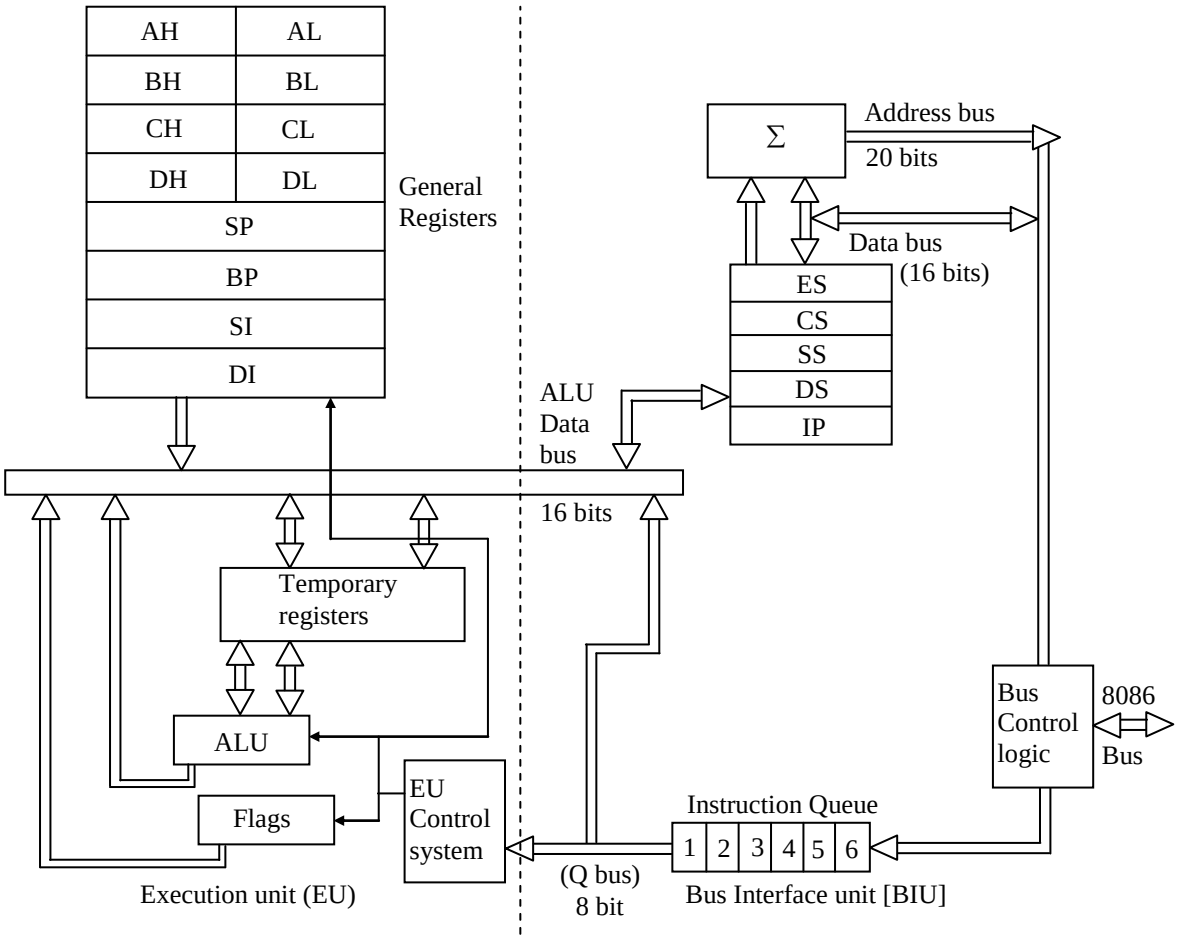
(v) Power dissipation:-

The power dissipation is another characteristic and it is a very important characteristic specially in the present scenario where the trend is to pack in large number of circuits in a given chip as many devices as possible in a given chip. We have millions of transistors nowadays in the VLSI chips, if we are introducing so many devices, the power dissipation is obviously going to up. So, in order to be able to integrate a larger number of circuits large number of components the power dissipation has to be brought down somehow.

Power dissipation = fCV_{dd}^2

Where f = frequency of operation
C = MOSFET capacitance
V_{dd} = Supply voltage.

06. (c)
Sol:



8086 has two blocks BIU and EU, BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands. The instruction bytes are transferred to the instruction queue. EU executes instructions from the instruction system byte queue.

Both BIU and EU operates asynchronously to give the 8086 an overlapping instruction fetch and execution mechanism which is called pipelining. This results in efficient use of the system bus and system performance. BIU contains instruction queue. Segment registers, instruction pointer, address adder. EU contains control circuitry, Instruction decoder, ALU, pointer and index register, flag register.

Bus interface unit (BIU):

It provides a full 16 bit bidirectional data bus and 20-bit address bus. BIU responsible for performing all external bus operations specifically it has the following functions:

Instruction fetch, instruction queuing, operand fetch and storage, address relocation and bus control BIU uses a mechanism known as an instruction stream queue to implement a "pipeline architecture". This queue permits prefetch of upto six bytes of instruction code.

Whenever the queue of the BIU is not full, it has room for at least two more bytes and at the same time the EU is not requesting it to read or write operations from memory, the BIU is free to look ahead in the program by fetching the next sequential instruction.

These prefetching instructions are held in its FIFO queue With it's 16 bit data bus, the BIU fetches two instruction bytes in a single memory cycle.

After a byte is loaded at the input end of the queue, it automatically shifts up through the FIFO to empty location nearest the output. The EU accesses the queue from the output end. It reads one instruction byte after the other from the output of the queue. If the queue is full and the EU is not requesting access to operand in memory. These intervals of no bus activity, which may occur between bus cycles are known as "idle state", If BIU is already in the process of fetching an instruction when the EU request it to read or write operands from memory or I/O, the BIU first completes the instruction fetch bus cycle before initiating the operand/write cycle.

BIU contains a decidated adder which is used to generate 20 bit physical address that is the output on the address bus. This address is formed by adding an appended 16 bit segment address and a 16 bit offset address. BIU is also responsible for generating bus control signals such as those for memory read or write and I/O read or write.

Execution Unit (EU):

EU is responsible for decoding and executing all instructions. The EU extracts instructions from the top of the queue in the BIU, decodes them. Generates operands if necessary passes them to the BIU and requests it to perform the read or write cycles to memory or I/O and perform the operation specified by the instruction on the operands.

During the execution of the instruction, the EU tests the status and control flags and updates them based on the results of executing the instruction.

If the queue is empty, the EU waits for the next instruction byte to be fetched and shifted to top of the queue.

07. (a)

Sol: Shunt motor

$V = 200V$

$I_{a_1} = 40\,A$

$R_a = 1\Omega$

$E_{b_1} = V - I_a R_a = 200 - 40 \times 1$

$= 160\ V$

$$\frac{E_{b_2}}{E_{b_1}} = \frac{N_2}{N_1} \times \frac{\phi_2}{\phi_1}$$

$E_{b_2} = 1.2 \times x \times E_{b_1}$

$E_{b_2} = 192x$

$= V - I_{a_2} R_a$

$192x = 200 - I_{a_2}.1$ .....(1)

$N_2 = 1.2\ N_1$

$T_2 = 1.1\ T_1$

Let $\frac{\phi_2}{\phi_1} = x$

$$\frac{T_2}{T_1} = \frac{\phi_2}{\phi_1} \times \frac{I_{a_2}}{I_{a_1}}$$

$$1.1 = x \times \frac{I_{a_2}}{40}$$

$$I_{a_2} = \frac{44}{x} \text{ ..... (2)}$$

$$192x = 200 - \frac{44}{x}$$

$$192x^2 - 200x + 44 = 0$$

$$x^2 - 1.04x + 0.229 = 0$$

$$x = \frac{1.04 \pm \sqrt{1.04^2 - 4 \times 0.11}}{2}$$

$$= \frac{1.04 \pm 0.411}{2}$$

$$= 0.725 \text{ or } 0.3145$$

$$x = 0.725$$

% reduction of field current = 27.5%

07. (b)

Sol:

(i) Coal and ash handling plant
(ii) Steam generator or Boiler
(iii) Super heater
(iv) Economizer
(v) Airpreheater.
(vi) Steam Turbine
(vii) Condenser
(viii) Cooling towers
(ix) Feed water heater
(x) A. C. Generator (or) Alternator
(xi) Exciter
(xii) Electro static precipitator

(i) Coal and Ash handling plant:

The coal is transported to the power station by road 'or' rail is stored in the coal storage plant. The coal is delivered to the coal handling plant. Where it is pulverized (i.e., crushed into small pieces) in order to increase its surface exposure. Thus promoting rapid combustion without using large quantity of excess air. The pulverized coal is fed to the boiler by belt conveyors.

(ii) Steam Generator (or) Boiler:

Boiler is a device, where in water is converted into steam by utilizing the heat of combustion
This is two types:

(A) Water tube boiler (B) Fire tube boiler

(A) Water tube boiler:

The water flows through the tubes and hot combustion gases flow over these tube, water tube boiler are used universally for such plant.

Features of water tube boiler.

i) Method of water circulation
ii) Improved method of heating
iii) Easy removal of scale from inside the tube.

(B) Fire Tube Boiler:

The hot combustion gases flow through the tube. Water is surrounded by the fire tube.

(iii) Super Heater:

A super heater is a device which raises the temperature of the steam much above the boiling point of water. Super heater heat is taken from flue gases. Normal radiant type of heat transfer method is used. It is placed between boiler and turbine. It improves efficiency of plant.

(iv) Economizer:

Economizer mainly consists of closely spaced parallel tubes through which feed water on its way to boiler flows and the flue gases flow outsides the tubes. Some of the heat energy of the flue gases is recovered by heating the feed water heater saturation but, not converted into steam this results saving (10-25%) and raising boiler efficiency.

(v) Airpreheater:

An airpreheater increases the temperature of the air supplied for coal burning by deriving heat from flue gases. Air is drawn from the atmosphere. By a forced draught fan and is passed through air preheated before supplying to the boiler furnace. Air pre heaters are placed in between economizer and chimney. The efficiency of boiler is increased.

(vi) Steam Turbine:

A steam turbine may be defined as a rotating machine, which converts the energy contained in steam into mechanical energy or rotary energy.

Basically there are two types of Turbines

(A) Impulse Turbine
(B) Reaction turbine
(C) Impulse Reaction Turbine (this turbine is a combination of impulse and reaction turbines)

(A) Impulse Turbine:

The steam expands completely in the stationary nozzles (or) fixed blades, the pressure over the moving blades remaining constant, so the steam attains a high velocity and impinges against the moving blades this results in the impulsive force on the moving blades which sets the rotor rotating.

(B) Reaction turbine:

The steam is partially expanded in the stationary nozzles, the remaining expansion takes place during its flow over the moving blades, the result is that the momentum of the steam causes a reaction force on the moving blades which sets the rotor in motion.

(vii) Condenser:

A condenser is a device which condenses the steam at the exhaust of Turbine. It serves two important functions. (1) It creates a very low pressure at the exhaust of Turbine, thus permitting expansion of the steam in the prime mover to a very low pressure. This helps in converting heat energy of steam into Mechanical energy in the prime mover. (2) The condensed steam can be used as feed water to the boiler. It is improves power plant efficiency.

(viii) Cooling Towers:

A condenser is a device in which exhaust steam from steam turbine is condensed and the heat energy given by the steam during condensation is taken up by the cooling tower.

(x) Generator:

- Each alternator is coupled to a steam turbine and converts mechanical energy of the turbine into electrical energy.
- Alternator used in thermal power plants are of usually 2 - pole (or) 4 - pole running at 3000 rpm (or) 1500 rpm for 50 Hz operation.

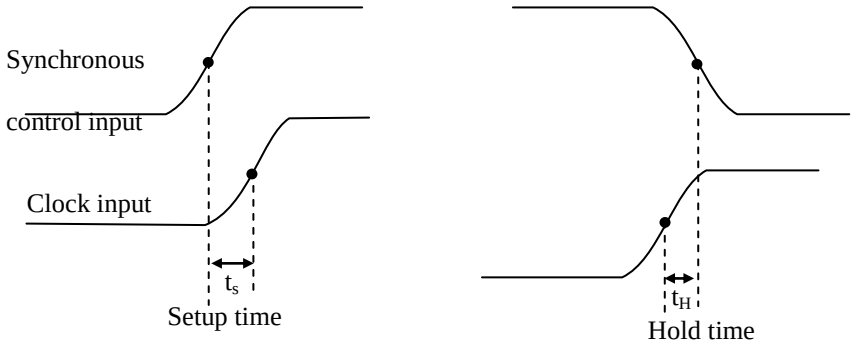
(xi) Exciter:

- Exciters are nothing but the D.C. Generators their main function is to supply dc power to the field system (rotor).
- Exciters are mounted on the same shaft of the alternator.
- The capacity of the exciter is about 0.5% to 3% of the main alternator capacity.
- In some cases a pilot exciter may be used to excite the main exciter itself.

(xiii) Electro static precipitator: The use of electrostatic precipitator is to remove fine, dust particles from flue gas. It is connected to high D.C. voltage about 30 kV. It is placed between combustion chamber and chimney

07. (c)

Sol: Two timing requirements must be met if a clocked FF is to respond reliably to its control inputs when the active clock transition occurs. These requirements are illustrated in figure shown below



Setup time:

Setup time, t_s is the time interval immediately preceding the active transition of the clock signal during which the control input must be maintained at the proper level. If this time requirement is not met, the FF may not respond reliably when the clock edge occurs.

Hold time:

Hold time, t_H is the time interval immediately following the active transition of the clock signal during which the synchronous control input must be maintained at the proper level. If this requirement is not met, the FF will not trigger reliably.

IC manufacturers usually specify the minimum allowable set up time $(t_s)_{min}$ and minimum acceptable value of hold time $t_{H(min)}$. Thus, to ensure that a clocked FF will respond properly when the active clock transition occurs, the control inputs must be stable (unchanging) for atleast a time interval equal to $t_{s(min)}$ prior to the clock transition, and for atleast a time interval equal to $t_{H(min)}$ after clock transition.

These timing requirements are very important in synchronous systems because, there will many situations where the synchronous control inputs to a FF are changing at approximately the same time as the clock input.

07. (d)

Sol: For a half-wave rectified sine wave,

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\alpha \times d\alpha$$

$$I_{dc} = \frac{1}{2\pi} \times I_m - \cos\alpha\,|_0^{\pi} = \frac{I_m}{\pi} \text{ ------ (i)}$$

Power delivered to the load

$$P_L = \frac{R_L}{T}\int_0^{T/2} I_m^2 \sin^2 \omega t dt$$

$$P_L = R_L \times \frac{I_m^2}{T}\int_0^{T/2} \frac{[1-\cos 2\omega t]}{2} dt$$

$$P_L = \frac{I_m^2}{2T} \times R_L \times \left[t - \frac{\sin 2\omega t}{2\omega}\right]_0^{T/2}$$

$$P_L = \frac{I_m^2 R_L}{4} \text{ ------- (ii)}$$

Using expression for I_m from equation (i) in equation (ii), we get,

$$P_L = \frac{(\pi I_{dc})^2 R_L}{4}$$

$$P_L = \frac{\pi^2 \times (10 \times 10^{-3})^2 \times 10^3}{4} = 0.246$$

08. (a)

Sol: $E_2 = 6.6$ kV $\Rightarrow E_{ph} = \dfrac{6.6\times10^3}{\sqrt{3}} = 3810$ V

(i) $E = \sqrt{(V\cos\phi + I_a R_a)^2 + (V\sin\phi - I_a X_s)^2}$

$3810 = \sqrt{(V \times 0.8 + 180 \times 0.6)^2 + (V \times 0.6 - 180 \times 6)^2}$

$\Rightarrow$ **V = 4256.65 V**

(ii) Voltage regulation $= \dfrac{E-V}{V}\times 100$

$= \dfrac{3810 - 4256.65}{4256.65}\times 100$

= – 10.49%

(iii) $E = V\angle 0 + I_a \angle \pm\phi \; Z_s\angle\theta$

$= 4256.65\angle 0 + 180\angle 36.86 \times (0.6+j6)$

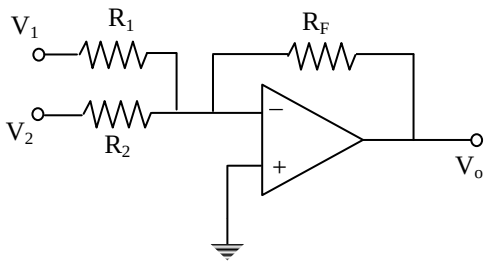
$= 3810\angle 14.1°$

$\therefore$ **δ = 14.1°**

08. (b)

Sol:

(i)



For the circuit shown above we have:

$$V_o = \left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2\right)$$

Since it is required that $V_o = -(V_1 + 5V_2)$.

We want to have:

$$\frac{R_F}{R_1} = 1 \text{ and } \frac{R_F}{R_2} = 5$$

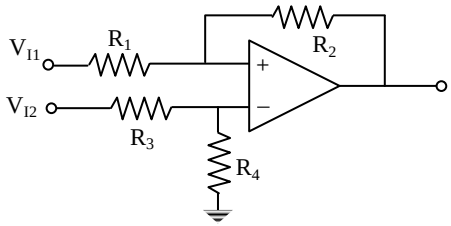
It is also desired that for a maximum output voltage of 10V, the current in the feedback resistor does not exceed 1mA.

$$\therefore \frac{10V}{R_F} \le 1mA \Rightarrow R_F = \frac{10V}{1mA} \Rightarrow R_F = 10k\Omega$$

Let us choose R_F to be 10kΩ, then

$$R_1 = R_F = 10k\Omega \text{ and } R_2 = \frac{R_F}{5} = 2k\Omega$$

(ii)



(A) $R_1 = R_3 = 2k\Omega$, $R_2 = R_4 = 200k\Omega$

Since $\frac{R_4}{R_3} = \frac{R_2}{R_1}$ we have:

$$A_d = \frac{V_o}{V_{i_1} - V_{i_2}} = \frac{R_2}{R_1} = \frac{200}{2} = 100V/V.$$

(B) $R_{id} = 2R_1 = 2 \times 2k\Omega = 4k\Omega$

Since we are assuming the op-amp is ideal

$R_o = 0\Omega$

(C) $A_{cm} = \frac{V_o}{V_{Icm}} = \left(\frac{R_4}{R_4 + R_3}\right)\left(1 - \frac{R_2}{R_1}.\frac{R_3}{R_4}\right)$

$$= \left(\frac{1}{1+\frac{R_3}{R_4}}\right)\left(1-\frac{R_2}{R_1}.\frac{R_3}{R_4}\right)$$

$$= \frac{\frac{R_4}{R_3}-\frac{R_2}{R_1}}{\frac{R_4}{R_3}+1}$$

The worst case common-mode gain, A_{cm} happens when $|A_{cm}|$ has its maximum value.
If the resistors have 1% tolerance, we have

$$\frac{R_4,\text{nom}(1-0.01)}{R_3,\text{nom}(1+0.01)} \le \frac{R_4}{R_3} \le \frac{R_4,\text{nom}(1+0.01)}{R_3,\text{nom}(1-0.01)}$$

Where, R_4, nom and R_3, nom are nominal values for R_4 & R_3
We have:

R_3,nom = 2kΩ and R_4, nom = 200kΩ, thus

$$\frac{200\times0.99}{2\times1.01} \le \frac{R_4}{R_3} \le \frac{200\times1.01}{2\times0.99}$$

$$98.02 \le \frac{R_4}{R_3} \le 102.02.$$

Similarly we can show that

$$98.02 \le \frac{R_2}{R_1} \le 102.02.$$

Hence, $-102.02 \le \frac{R_2}{R_1} \le -98.02$

Therefore,

$$-4 \le \frac{R_4}{R_3}-\frac{R_2}{R_1} \le 4 \Rightarrow \left|\frac{R_4}{R_3}-\frac{R_2}{R_1}\right| \le 4$$

In the worst case

$$\frac{\left|\frac{R_4}{R_3}-\frac{R_2}{R_1}\right|}{1+\frac{R_4}{R_3}} \le \frac{4}{1+98.02} \Rightarrow |A_{cm}| \le 4.04$$

Note that worst case A_{cm} can happen when

$$\frac{R_4}{R_3} = 98.02 \text{ and } \frac{R_2}{R_1} = 102.02$$

The differential gain (A_d) of the amplifier is

$$A_d = \frac{R_2}{R_1},$$

$$\text{CMRR} = 20\log\frac{|A_d|}{|A_{cm}|} = 20\log\frac{102.02}{0.04} = 68\,\text{dB}$$

(iii) We choose $R_3 = R_1$ and $R_4 = R_2$. Then for the circuit to behave as a difference amplifier with a gain of 10 and an input resistance of 20kΩ, we require

$A_d = \frac{R_2}{R_1} = 10$ and

$R_{id} = 2R_1 = 20k\Omega \Rightarrow R_1 = 10k\Omega$ and

$R_2 = A_d.R_1 = 10 \times 10k\Omega = 100k\Omega$

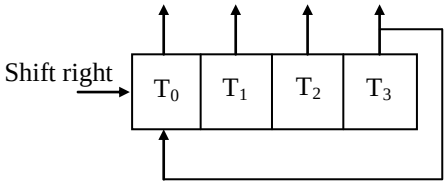
$\therefore R_1 = R_3 = 10k\Omega$ and

$R_2 = R_4 = 100k\Omega$

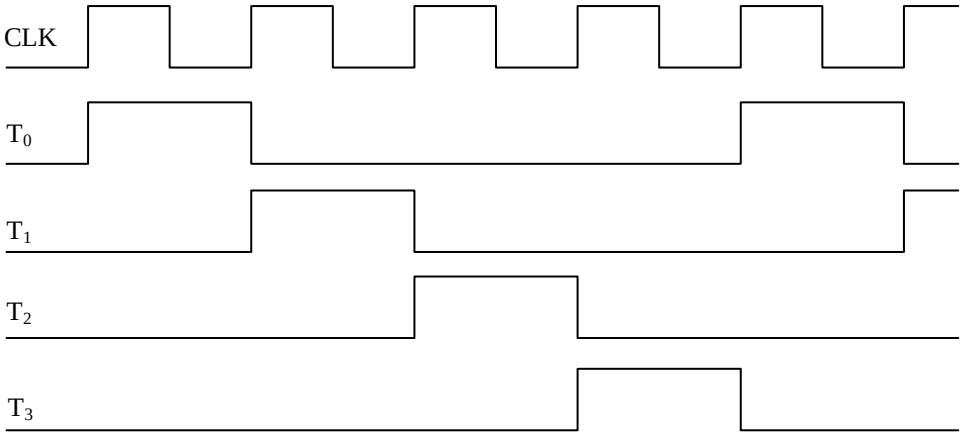
08. (c)

Sol: Ring counter:

A ring counter is a circular shift register with only one flip-flop being set at any particular time, all others are cleared. The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals below figure shows a 4-bit shift register connected as a ring counter.

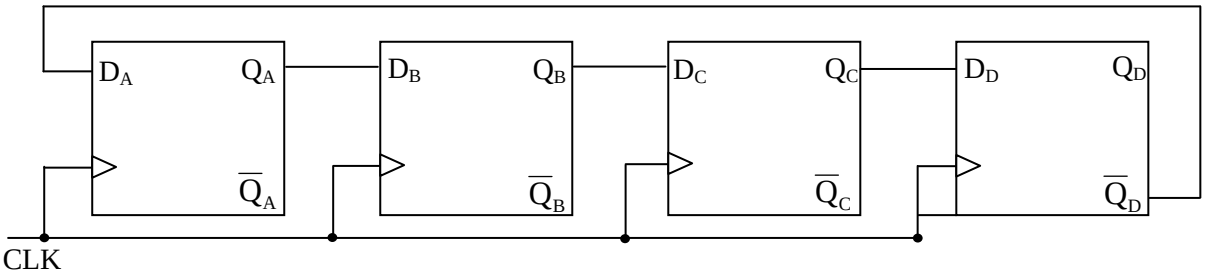


Let the initial value of the register is 1000. The single bit is shifted right with every clock pulse and circulates back from T_3 to T_0. Each flip-flop is in the 1 state once every four clock cycles and produces one of the four timing signals shown below. A n-bit ring counter goes through a sequence of n states.



Johnson Counter:-

A k-bit ring counter circulates a single bit among the flip-flops to provide k distinguishable states. The number of states can be doubled if the shift register is connected as a switch tail ring counter. A switch tail ring counter is a circular shift register with the complement output of the last flip-flop connected to the input of the first flip-flop. Johnson counter [switch tail ring counter] shown in below figure.



The circular connection is made from the complement output of the rightmost flip-flop to the input of the leftmost flip-flop. The register shifts its contents once to the right with every clock pulse, and at the same time, the complement value of the D-flip flop is transferred into A flip-flop. Starting from cleared state, a 4-bit Johnson counter goes through a sequence of eight states.
In general, a k-bit switch-tail ring counter will go through a sequence of 2k states.

Clock	Flip-Flop outputs			
	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0