ACE Engineering Academy

TEST ID: 307

Head Office : Sree Sindhi Guru Sangat Sabha Association, # 4-1-1236/1/A, King Koti, Abids, Hyderabad – 500001.

Ph: 040-23234418, 040-23234419, 040-23234420, 040 - 24750437

Hyderabad | Delhi | Bhopal | Pune | Bhubaneswar | Lucknow | Patna | Bengaluru | Chennai | Vijayawada | Vizag | Tirupati | Kukatpally | Kolkata | Ahmedabad

# ESE- 2019 (Prelims) - Offline Test Series Test-13

## ELECTRICAL ENGINEERING

## SUBJECT: CONTROL SYSTEMS, ANALOG ELECTRONICS AND DIGITAL ELECTRONICS & BASIC ELECTRONICS ENGINEERING

## SOLUTIONS

**01. Ans: (a)**

**Sol:** Number of forward paths = 4

$Rx_1x_2x_3x_4C$

$Rx_1x_3x_4C$

$Rx_1x_2x_4C$

$Rx_1x_3x_2x_4C$

Number of loops = 5

$x_1x_2x_4x_1$

$x_2x_3x_2$

$x_1x_3x_4x_1$

x1x2 $x_3$x4x1

$x_1x_3x_2x_4x_1$

**02. Ans: (c)**

**Sol:** $S_K^T = \frac{\partial T}{\partial K}\frac{K}{T}$

$$= \frac{\partial}{\partial K}\left(\frac{1+3K}{1+2K}\right)\frac{K}{\left(\frac{1+3K}{1+2K}\right)}$$

$$= \left[\frac{(1+2K)3-(1+3K)2}{(1+2K)^2}\right]\frac{K(1+2K)}{1+3K}$$

$$= \frac{K}{(1+3K)(1+2K)}$$

$$= \frac{K}{1+5K+6K^2}$$

Substitute K = 1

$$S_K^T = \frac{1}{12}$$

**03. Ans: (d)**

**Sol:** $c(t) = L^{-1}[R(s).G_2(s)]$

$$= L^{-1}\left[\frac{1}{s}.\frac{1}{s+2}\right]$$

$= 0.5\,(1 - e^{-2t})\,u(t)$

**04. Ans: (c)**

**Sol:** $CE = s^4 + 2s^2 + 3 = 0$

| | | | |
|---|---|---|---|
| $s^4$ | 1 | 2 | 3 |
| $s^3$ | 0(4) | 0(4) | 0 |
| $s^2$ | 1 | 3 | |
| $s^1$ | –8 | 0 | |
| $s^0$ | 3 | | |

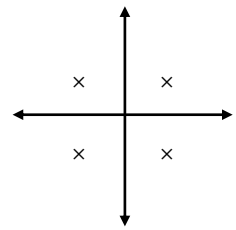
Given equation is AE, $\frac{dAE}{ds} = 4s^3 + 4s = 0$

Number of sign changes below the AE = 2

Number of RHP = Number of LHP = 2

Number of $j\omega P = 0$

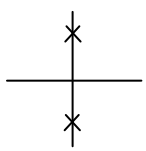
The four poles are located in quadrate as shown below



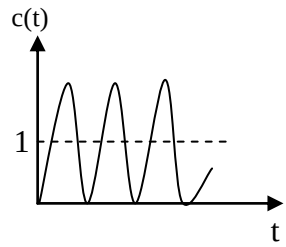
**05. Ans: (a)**

**Sol: Location of poles** **Unit step response**

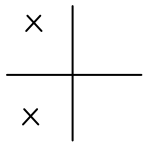
(A)



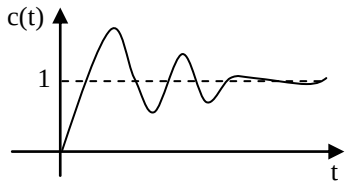
(4)



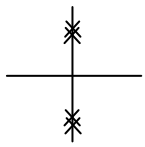

(B)



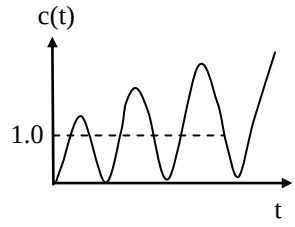
(1)



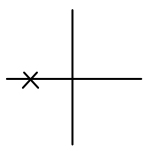

(C)



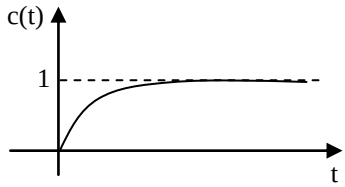
(2)




(D)



(3)



**06. Ans: (c)**

**Sol:** $$\frac{V_o(s)}{V_i(s)} = \frac{\left[\frac{1}{Cs}\right]\left[\frac{1}{Cs}\right]}{R\left[R+\frac{1}{Cs}+\frac{1}{Cs}\right]+\frac{1}{Cs}\left[R+\frac{1}{Cs}\right]}$$

Substitute R = 1Ω, C = 1F

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{s^2+3s+1}$$

**07. Ans: (c)**

**Sol:** C(s) = TF×R(s)

$$R(s) = L[\cos t] = \frac{s}{s^2+1}$$

$$C(s) = \frac{1}{s^2}\cdot\frac{s}{s^2+1}$$

$$= \frac{1}{s(s^2+1)} = \frac{1}{s}+\frac{-s}{s^2+1}$$

$$c(t) = L^{-1}[C(s)] = 1-\cos t$$

**08. Ans: (d)**

**Sol:** Noise transfer function

$$\frac{C(s)}{N(s)} = \frac{G_1}{1-(-2G_1G_2H)} = \frac{G_1}{2G_2G_1H+1}$$

**09. Ans: (b)**

**Sol:** From option (b)

$\omega = 0 \ldots\ldots \angle\phi = -270°$

$\omega = \infty \ldots\ldots \angle\phi = -180°$

At $\omega = 0$; $\angle\phi = -270^o$

i.e., 3-poles at origin

**10. Ans: (b)**

**Sol:** $$\left|\frac{k}{s^2}\right|_{\omega=10} = 1$$

$$\frac{k}{\omega^2} = 1$$

$$k = \omega^2 = 10^2$$

$\therefore K_a = k = 100$

**11. Ans: (a)**

**Sol:** The number of loops = 4

Loop gains = 1, 1, 1, –1

$\therefore$ Sum of individual loop gains =1+1+1 – 1

= 2

**12. Ans: (b)**

**Sol:** $$PM = 180° + \angle\frac{j\omega+1}{(j\omega)^2\sqrt{2}}\Bigg|_{\omega=\omega_{gc}}$$

$$\left|\frac{j\omega_{gc}+1}{(j\omega_{gc})^2\sqrt{2}}\right| = \frac{\sqrt{\omega_{gc}^{\ 2}+1}}{\omega_{gc}^2\sqrt{2}} = 1$$

$\omega_{gc} = 1$rad/sec

$\therefore$ PM = $180° + \tan^{-1}\omega_{gc} - 180°$

PM = 45°

**13. Ans: (c)**

**Sol:** For region 1 N = –1

For region 2 N = –2

For region 3 N = 0

Given,

P = 0, Z = 0

$\therefore$ N = P – Z = 0

Only if (–1, j0) lies in region (3) N is zero

**14. Ans: (a)**

**Sol:** A derivative controller

$\rightarrow$ improves the stability of the system

$\rightarrow$ improves phase margin

$\rightarrow$ decreases over shoot

$\rightarrow$ decreases settling time

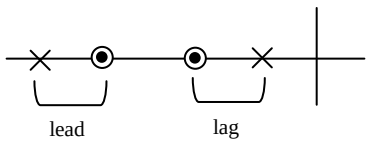
**15. Ans: (b)**

**Sol:** Transfer function of lag-lead compensator is

$$G_c(s) = \frac{(s+Z_1)(s+Z_2)}{(s+P_1)(s+P_2)}$$

Where $P_1 < Z_1 < Z_2 < P_2$

Pole zero plot of lag-lead compensator




**16. Ans: (b)**

**Sol:** $k_p = \underset{s\to 0}{Lt}\, G(s) = \infty$

$k_v = \underset{s\to 0}{Lt}\, s\,G(s) = \infty$

$k_a = \underset{s\to 0}{Lt}\, s^2 G(s) = 10$

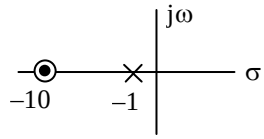
Error due to $1 + t + \frac{t^2}{2} = \frac{1}{1+k_p} + \frac{1}{k_v} + \frac{1}{k_a}$

$= 0.1$

**17. Ans: (b)**

**Sol:** Let $G_c(s) = \frac{1+s/10}{1+s/1}$

Pole zero plot of lag compensator




**18. Ans: (c)**

**Sol:** Given positive feedback system

$\therefore$ Characteristic equation 1 – G(s)H(s) = 0

$$1 - \frac{k}{s-6} = 0$$

$$s - 6 - k = 0$$

$$s - (k + 6) = 0$$

$$k + 6 < 0$$

$$k < -6$$

**19. Ans: (c)**

**Sol:** $G(s)\,H(s) = \frac{k}{s(s+1)(s+2)}$

CE = 1 + G(s)H(s) = 0

s(s+1)(s+2) + k = 0

$s^3 + 3s^2 + 2s + k = 0$

| | | |
|---|---|---|
| $s^3$ | 1 | 2 |
| $s^2$ | 3 | k |
| $s^1$ | $\frac{6-k}{3}$ | 0 |
| $s^0$ | k | |

$k_{marginal} = 6$

$\therefore$ The value of k at point A = 6

**20. Ans: (b)**

**Sol:** Every branch of the RLD starts at a pole (k = 0), and terminates at a zero (k = ∞) of the OLTF G(s)H(s).

On the real axis to the right side of any section, if the sum of total no. of open loop poles and zeros are odd, RLD exists in that section.

**21. Ans: (d)**

**Sol:** $\frac{C(s)}{R(s)} = T(s) = \frac{(s+2)e^{-s}}{(s^2+4)}$

Impulse response = $L^{-1}$ (T(s))

$$T(s) = \frac{se^{-s}}{s^2+4} + \frac{2e^{-s}}{s^2+4}$$

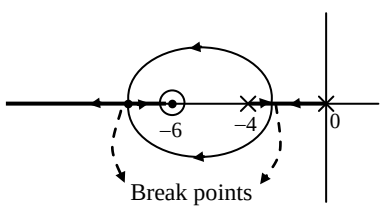
$IR = L^{-1}(T(s))$

$$IR = L^{-1}\left[\frac{se^{-s}}{s^2+4}\right] + L^{-1}\left[\frac{2e^{-s}}{s^2+4}\right]$$

$IR = \cos 2(t-1) + \sin 2(t-1)$

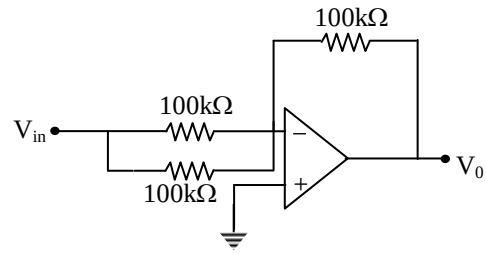
**22. Ans: (b)**

**Sol:**




**23. Ans: (c)**

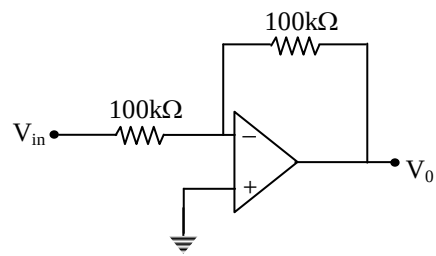
**Sol:** When the switch (S/W) is on:




$$V_0 = -\frac{R_f}{R} = -\frac{100\,k}{100\,k\,//\,100\,k} \times V_{in}$$

$$\frac{V_0}{V_{in}} = -2 \Rightarrow X = -2$$

When the switch is OFF:




$$\frac{V_0}{V_{in}} = \frac{-100k}{100k} = -1$$

$\Rightarrow Y = -1$

$X = -2, Y = -1$

$X = -1 - 1$

$X = Y - 1$

**24. Ans: (c)**

**Sol:** If the emitter bypass capacitor in a common emitter amplifier is removed,

i) The input resistance of the amplifier will be increased

ii) The voltage gain of the amplifier will be decreased.

**25. Ans: (c)**

**Sol:** During positive half-cycle of input voltage,

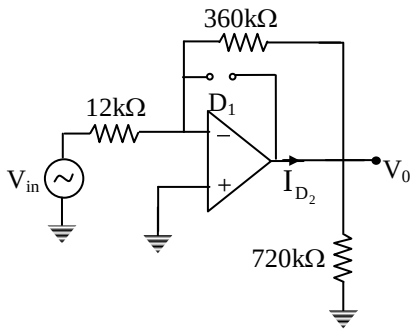
$D_1 \rightarrow$ ON

$D_2 \rightarrow$ OFF $\Rightarrow I_{D_2} = 0$

During negative half-cycle of input voltage,

$D_1 \rightarrow$ OFF

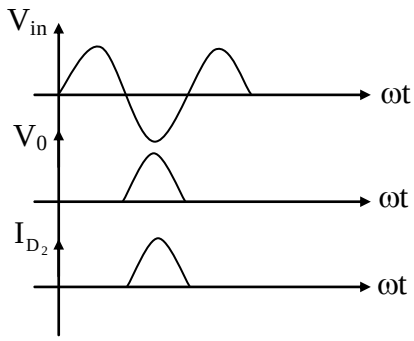
$D_2 \rightarrow$ ON




$V_0 = -30V_{in}$ and $V_{in} = -2\sin\omega t$

$\therefore V_0 = 60\sin\omega t$

The output voltage waveforms are shown below



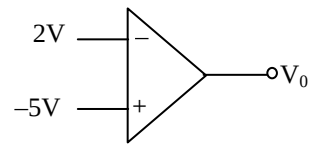

$$I_{D2} = \frac{V_0}{720k} + \frac{V_0}{360k}$$

$$= \frac{V_0}{240k} = 0.25\sin\omega t \text{ mA when } V_{in} < 0$$

$$\text{RMS value of } I_{D2} = \frac{0.25}{2} = 0.125\text{mA}$$

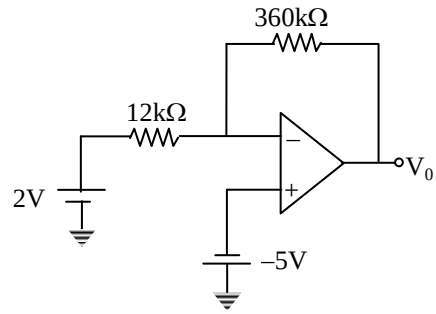
**26. Ans: (c)**

**Sol:** Open loop configuration:




$V_0 = (-5 - 2)\, A_0 \Rightarrow -Ve$

$\therefore D_1 \rightarrow$ OFF; $D_2$ is ON




$V_0 = -215$ V

$|V_0| \geq |-12|$

$\Rightarrow V_0 = -12$ V

ACE

# SUMMER

## SHORT TERM BATCHES

Start Early.. Gain Surely..

SHORT TERM BATCHES

### GATE+PSUs - 2020

Admissions Open From 14th NOV 2018

**HYDERABAD**

29th April | 06th May | 11th May

18th May | 26th May | 02nd June 2019

**DELHI**

11th May | 23rd May 2019

**EARLY BIRD OFFER :**

Register on or Before 31st December 2018 : 5000/- Off | Register on or Before 31st March 2019 : 3000/- Off

ACE

# TEST YOUR PREP

IN A REAL TEST ENVIRONMENT

## Pre GATE - 2019

Date of Exam : **20th January 2019**

Last Date to Apply : **31st December 2018**

**Highlights :**

- Get real-time experience of **GATE-2019** test pattern and environment.
- Virtual calculator will be enabled.
- Post exam learning analytics and All India Rank will be provided.
- Post GATE guidance sessions by experts.
- Encouraging awards for **GATE-2019** toppers.

**27. Ans: (c)**

**Sol:** 1. p-n junction diode is a passive component

2. $W \propto V_j^{1/n}$ ( n = 2 for non-linear junction

n =3 for linear junction) and

$V_j = V_0 - V_B \rightarrow$ For forward biasing

3. $I_{02} = I_{01} \times 2^{\frac{T_2 - T_1}{10}}$ (reverse saturation current increases with increasing in temperature)

So statement (2) and (3) are correct and (1) is false.

**28. Ans: (b)**

**Sol:** $-V_{D2} + V_{D1} + V = 0$

$V = V_{D2} - V_{D1} = 50mV$

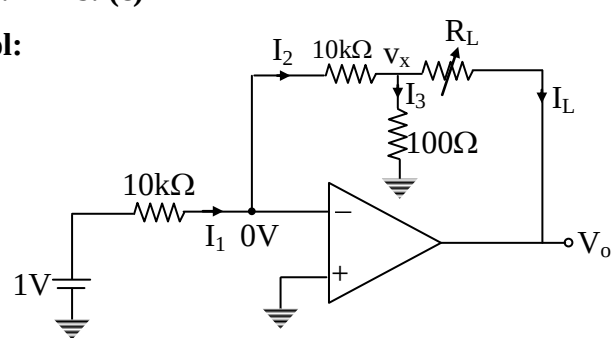
$10mV = I_1 + I_2$

$$\frac{I_2}{I_1} = \frac{I_s e^{\frac{V_{D2}}{V_T}}}{I_s e^{\frac{V_{D1}}{V_T}}} = e^{\frac{V_{D2}-V_{D1}}{V_T}}$$

$$\frac{I_2}{I_1} = e^{\frac{50mV}{25mV}} = e^2$$

**29. Ans: (c)**

**Sol:**




$$I_1 = \frac{1}{10k} = 0.1mA$$

$I_2 = I_1 = 0.1mA$

$(10k\ I_2) + (100\ I_3) = 0$

$$I_3 = \frac{-10k \times 0.1m}{100} = -10mA$$

$V_x = -100 \times 10m$

$V_x = -1V;$

$I_L = I_2 - I_3$

$= 10.1mA$

$V_0 = V_x - I_L R_L$

$V_0 = -1 - 10.1m\ R_L$

When $R_L = 100\Omega$

$\rightarrow V_{0max} = -1 - (10.1\times10^{-3}\times100)$

$= -2.01V$

When $R_L = 1k\Omega$

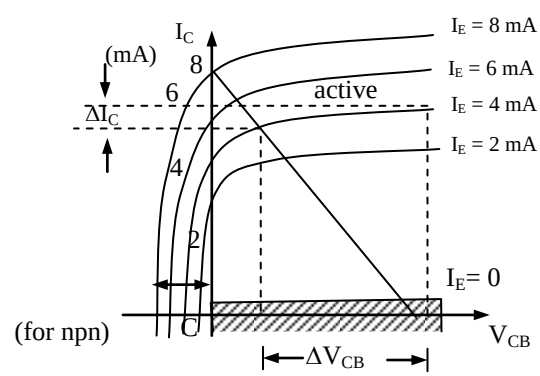
$\rightarrow V_{0min} = -1 - (10.1\times10^{-3}\times10^{3})$

$= -11.1V$

$-11.1V < V_0 < -2.01V$

**30. Ans: (c)**

**Sol**: **Output Characteristics: $I_C$ vs $V_{CB}|I_E$**



**Saturation Region:**

- Saturation region is the region left side to $V_{CB} = 0$ line.
- In saturation region, emitter and collector junction are in forward bias.
- In saturation region, collector current increases exponentially.
- It can be used as ON switch in saturation region.

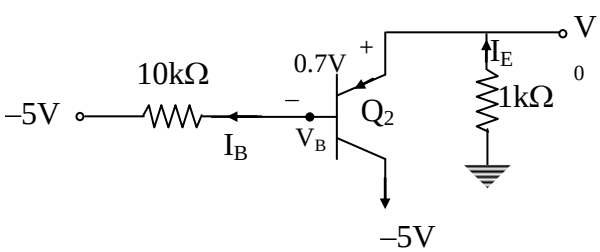
**31. Ans: (c)**

**Sol:** The emitter capacitance ($C_E$)is increases the gain $\left(\frac{V_0}{V_s}\right)$ and input resistance ($R_{in}$) decreases for AC signals.

**32. Ans: (b)**

**Sol:** For $V_i = -5V$

($Q_2$) gets ON, ($Q_1$) gets OFF




$Q_2$ is in active region

$V_B = V_0 - 0.7$

Apply KVL

$I_E + 0.7 + 10I_B - 5 = 0$

$$I_E + 10\left(\frac{I_E}{100}\right) = 5 - 0.7$$

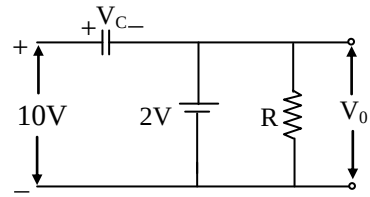
$$I_E = \frac{4.3}{1.1} = 3.9\text{mA}$$

$V_0 = -I_E(1k) = -3.9$ V

**33. Ans: (c)**

**Sol:** When $V_i = +10V$, diode is forward biased

$\therefore V_0 = 2V$

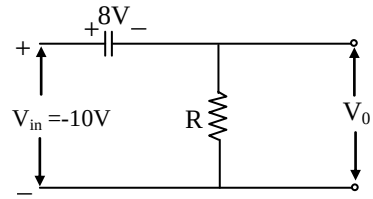



$-10 - V_C - V_0 = 0$

$10 - V_C - 2 = 0$

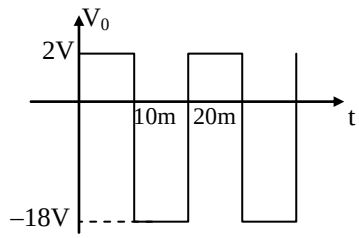
$V_C = +8V$

When $V_{in} = -10V$, diode is reverse biased.




$-10 - 8 = V_0 \Rightarrow V_0 = -18V$

**The output wave form:**



Average output voltage,

$$V_0 = \frac{2\times 10m - 18\times 10m}{20m} = -8V$$

**34. Ans: (c)**

**Sol:** In E-MOSFET

$V_{GS} = 0$ then $I_D = 0$

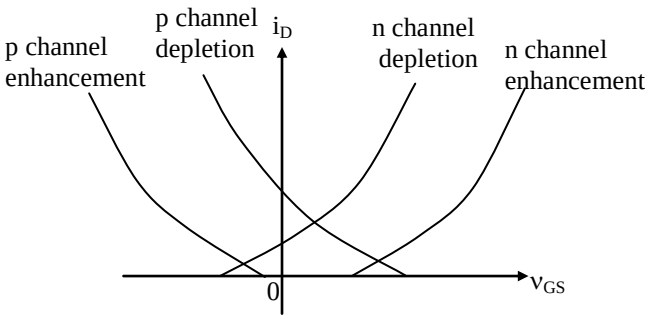
If $+V_{GS}$ increases then '$I_D$' also Increases

**35. Ans: (c)**

**Sol:** The phase of loop gain should be zero. So statement (ii) is wrong.

**36. Ans: (c)**

**Sol:**




$\therefore$ P- III, Q-II, R-IV, S-I

**37. Ans: (c)**

**Sol:** Overall voltage gain = product of individual voltage gains = 25×10×4 = 1000

Overall gain in dB = $20 \log_{10} 1000 = 60dB$

**38. Ans: (a)**

**Sol:** Given that, $\frac{dA}{A} = \frac{10}{100} = 0.1$

Variation in closed loop gain

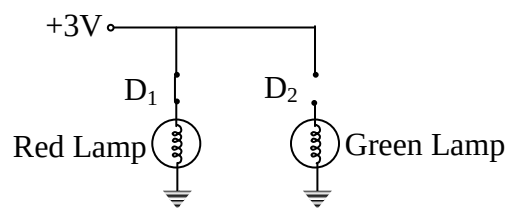
$$\frac{dA_f}{A_f} = \frac{0.1}{100} = 0.001$$

$$\text{Sensitivity factor} = \frac{1}{1+A\beta}$$

$$\text{Desensitivity factor} = \frac{1}{\text{Sensitivity}} = 1+A\beta$$

**39. Ans: (b)**

**Sol:** For $V_i = 3V$, $D_1$ is in forward bias, $D_2$ is in reverse bias

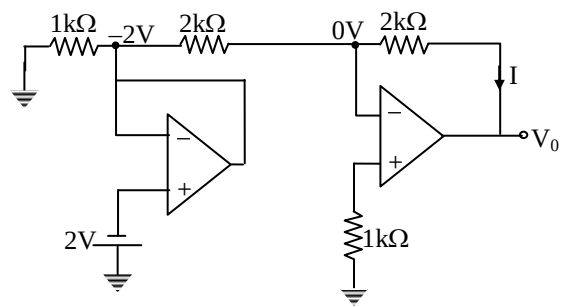



$\therefore$ RED lamp gets ON

GREEN lamp gets OFF

**40. Ans: (c)**

**Sol:** By open-loop comparator, $D_1$ is ON and $D_2$ is OFF



$$\frac{0+2}{2k}+\frac{0-V_0}{2k}=0$$

$$V_0 = 2V$$

The current through resistor,

$$I=\frac{-2}{2k}=-1mA$$

**41. Ans: (d)**

**Sol:** Let $I_1$ be current flowing through the resistor $R_c$

$I_1 = I_E = I_C + I_B = (\beta+1)I_B = 50I_B$

$$I_B=\frac{V_{CE}-V_{BE}}{R}=\frac{5-0.7}{R}=\frac{4.3V}{R}$$

Now, taking KVL in the collector-emitter circuit and using the above result.

$I_1R_C + I_ER_E = V_{CC} - V_{CE}$

$$\Rightarrow 50\times\left(\frac{4.3V}{R}\right)(7K+250\Omega)=20-5=15V$$

$$\Rightarrow R=\frac{50\times4.3\times7.25K}{15}=104k\Omega$$

**42. Ans: (a)**

**Sol:** $\sigma_p=(n\mu_n+p\mu_p)q$

$$=\left(\frac{n_i^2}{n_i\left(\frac{\mu_n}{\mu_p}\right)}\mu_n+n_i\left(\frac{\mu_n}{\mu_p}\right).\mu_p\right)q$$

$$=(n_i\mu_p+n_i\mu_n).q=\sigma_i$$

**43. Ans: (d)**

**Sol:** $\sigma=q(n\mu_n+p\mu_p)=q\left(n\mu_n+\mu_p\frac{n_i^2}{n}\right)$

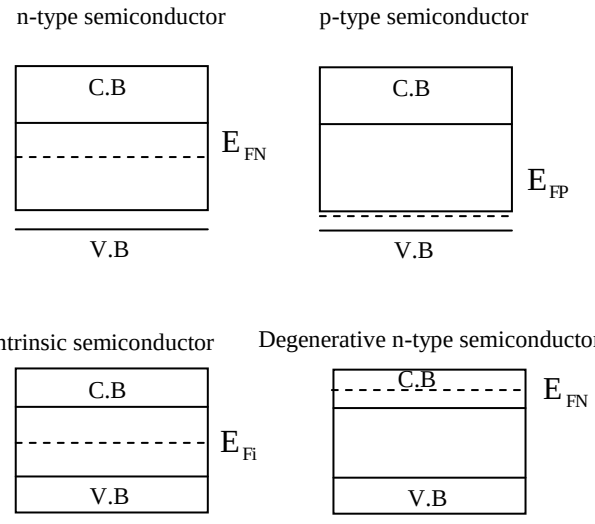
$$\frac{d\sigma}{dn}=q\left(\mu_n-\mu_p\frac{n_i^2}{n^2}\right)$$

Equate $\frac{d\sigma}{dn}$ to zero for minimum conductivity

$$n^2=n_i^2\frac{\mu_p}{\mu_n}\Rightarrow n=n_i\sqrt{\frac{\mu_p}{\mu_n}}$$

**44. Ans: (b)**

**Sol:**




**45. Ans: (a)**

**Sol:**

| | |
|---|---|
| 2 | 47 |
| 2 | 23–1 |
| 2 | 11–1 |
| 2 | 5 – 1 |
| 2 | 2 – 1 |
| | 1 – 0 |

+47 = 0 0 1 0 1 1 1 1

magnitude

sign

**46. Ans: (b)**

**Sol:** If $V_{in} > V_{out}$ set next bit

If $V_{in} < V_{out}$ set bit is going to reset and will set next bit

Here given that,

Analog input ($V_{in}$) = 6.2V

Digital output is greater than 6.2V so reset the last set bit and set the next bit.

Given digital input is equal to 11010000

$\therefore$ next value of SAR is 11001000

**47. Ans: (c)**

**Sol:** The maximum number of Boolean functions with

'n' variables = $2^{2^n}$

For '5' variables = $2^{2^5} = 2^{32}$ = 4294967296

**48. Ans: (b)**

**Sol:** 1) Without using any additional logic gates, we cannot implement any function (boolean function of more than one variable) using decoder.

2) Any function can be implemented using suitable MUX.

3) MUX is producing only one output, it cannot be used for multiple output function.

**49. Ans: (b)**

**Sol:** f(A,B,C,D) = $\prod$M(0,4,5,7,12,15)

= $\Sigma$m (1,2,3,6,8,9,10,11,13,14)

| A B / $S_1$ $S_0$ | $I_0$ 0 0 | $I_1$ 0 1 | $I_2$ 1 0 | $I_3$ 1 1 |
|---|---|---|---|---|
| $\overline{C}\overline{D}$ (00) | 0 | 4 | (8) | 12 |
| $\overline{C}D$ (01) | (1) | 5 | (9) | (13) |
| $C\overline{D}$ (10) | (2) | (6) | (10) | (14) |
| CD (11) | (3) | 7 | (11) | 15 |
| | C+D | $C\overline{D}$ | 1 | C⊕D |

$I_0 = C + D$

$I_1 = C\overline{D}$

$I_2 = 1$

$I_3 = C \oplus D$

**50. Ans: (d)**

**Sol**

$$f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}BCD + A\overline{B}CD + ABCD$$

= $\Sigma$m(0, 1, 2, 3, 7, 11, 15)

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | | | 1 | |
| 11 | | | 1 | |
| 10 | | | 1 | |

The simplified form of f(A, B, C, D)

$= \overline{A}\,\overline{B} + CD$

**51. Ans: (c)**

**Sol:** $(63)_{16} + (37)_{16} = (9A)_{16}$

$\therefore Y = 9A\ H$

**52. Ans: (b)**

**Sol:** It is up counter

All the flip flops are clearing when $Q_2\ Q_1 = 11$

0 0 0
0 0 1
0 1 0
0 1 1
1 0 0 $\Rightarrow$ 0 0 0

As it is asynchronous counter 100 state is overwriting with 000.

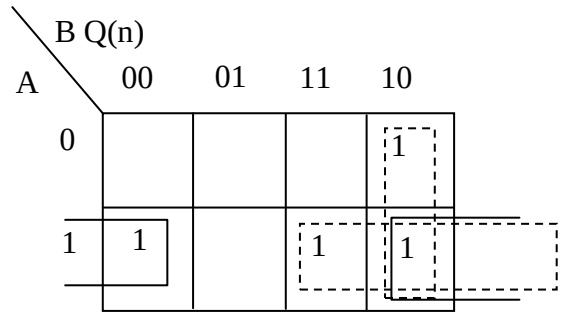
So it is counting only 4 states

**53. Ans: (a)**

**Sol:**

| A | B | Q(n+1) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | $\overline{Q(n)}$ |
| 1 | 0 | $\overline{Q(n)}$ |
| 1 | 1 | 1 |

| | A | B | Q(n) | Q(n+1) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 |




**54. Ans: (d)** $Q(n+1) = A\overline{Q(n)} + B\overline{Q(n)} + AB$

Sol. The 10's complement of decimal number = 9's complement + 1

$$\begin{array}{rr} & 9999\ .\ 99999 \\ (-) & 6091\ .\ 20100 \\ \hline 9\text{'s complement} \Rightarrow & 3908\ .\ 79899 \\ (+) & \underline{\qquad\qquad 1} \\ 10\text{'s complement} \Rightarrow & 3908\ .\ 79900 \end{array}$$

**55. Ans: (c)**

**Sol:**

$\overline{A}$

| BC \ DE | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | | |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | `1 | 1 |

A

| BC \ DE | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | | |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

Total number of minterms = 26

ACE

Launching

**Spark Batches** for

# ESE / GATE - 2020

from Mid May 2019

Admissions from **January 1st, 2019**

# @ DELHI

ACE

Launching

**Regular Batches** for

# ESE / GATE - 2020

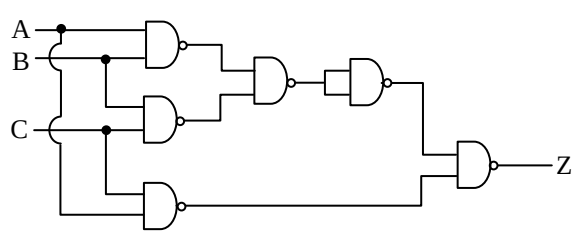
from Mid May 2019

Admissions from **January 1st, 2019**

# @ BHOPAL & LUCKNOW

**56. Ans: (c)**

**Sol:**




$f = AB + BC + AC$

$= \overline{\overline{AB + BC + AC}}$

$= \overline{\overline{AB}.\overline{BC}.\overline{AC}}$

$= \overline{\overline{\overline{AB}.\overline{BC}}.\overline{AC}}$

The function requires minimum 6 number of NAND gates to be realized.

**57. Ans:** (c)

**Sol:** BCD to 7 segment ---combinational circuit

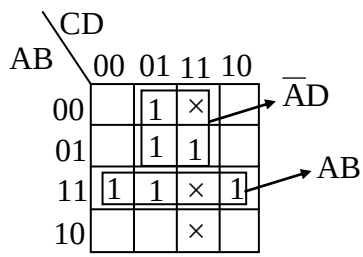
4 to 1 multiplexer ---- combinational circuit

4 bit shift register --- sequential circuit

BCD counter ---- sequential circuit

**58. Ans:(c)**

**Sol:** $f(A,B,C,D) = \Sigma m(1, 5, 7, 12, 13, 14)+d(3, 11, 15)$




$f(A,B,C,D) = AB + \overline{A}D$

For the input 0011, f=(0.0)+(1.1)=1

For the input 1011, f=(1.0)+(0.1)=0

**59. Ans: (b)**

**Sol:** (A) XTHL: Exchanges the contents of H and L registers with top of stack.

It takes 5 machine cycles = 16T states

(B) PUSH B: The contents of the register pair designated in the operand are copied onto the stack in the following sequence. The stack pointer register is decremented and the contents of the high order register (B) are copied into the location. The stack pointer register is decremented again and the contents of the low-order register (C) are copied to that location.

3 Machine cycles = 12 T-states

(C) HLT: Halt and enter into wait state

It takes 5 T-states.

(D) XCHG: The contents of the register H are exchanged with the contents of register D, and the contents of register L are exchanged with the contents of register E.

1-Fetch machine cycle = 4T states

**60. Ans: (c)**

**Sol:** 1) Registers are made of edge triggered flops where as latches are made from level triggered flip flops.

2) Latch employs cross coupled feed back connections.
3) Noise immunity is the amount of noise which can be applied at the input of the gate without causing the gate to change state.
4) Propagation delay is the time required for a gate to change its state.

**61. Ans: (c)**

**Sol:** $S_1$: Flash ADC is fastest ADC.

$S_2$: The most widely used ADC in multimeter is Successive approximation ADC.

$S_3$: The conversion time for Successive approximation ADC depends only on number of output bits. It doesn't depends on applied input voltage.

$S_4$: In dual slope ADC integrator is used.

**62. Ans: (d)**

**Sol:**

| | | |
|---|---|---|
| MVI | A, $06_H$ | ; [A] = 06H = $00000110_2$ |
| RLC | | ; [A] = $00001100_2$ = 0CH |
| MOV | B, A | ; [B] = 0CH = $00001100_2$ |
| RLC | | ; [A] = $00011000_2$ |
| RLC | | ; [A] = $00110000_2$ = 30H |
| ADD | B | [A] = [A]+[B] = 30H + 0CH = 3CH |
| HLT | | |

**63. Ans: (c)**

**Sol:** $T_0 = 2\times10^{-4}$ sec

$$f_0 = \frac{1}{T_0} = 5\text{kHz}$$

$$f_m = 3f_0 = 15\text{kHz}$$

$$\therefore \beta_{FM} = \frac{\Delta f_{MAX}}{f_{MAX}} = \frac{k_f A_m}{f_m}$$

$$= \frac{10^5\times1}{15\times10^3} = \frac{100}{15} > 1$$

$\therefore$ WBFM signal

$$BW_{FM} = 2(\beta + 1)f_m$$

$$= 2\left[\frac{115}{15}\right]\times15\times10^3$$

$BW_{FM}$ = 230 kHz

**64. Ans: (a)**

**Sol:** $\beta = \dfrac{\Delta f_{max}}{f_{max}}$

$f_{max}$ = 1000 Hz

$$\Delta f_i(t) = \frac{1}{2\pi}\frac{d}{dt}[\Delta\theta_i(t)]$$

$$= \frac{1}{2\pi}\frac{d}{dt}[5\sin3000t + 10\sin2000\pi t]$$

$$\Delta f_i(t) = \frac{1}{2\pi}[15000\cos3000t + 20000\pi\cos2000\pi t]$$

$$\Delta f_i(t)_{max} = \frac{1}{2\pi}[15000 + 20000\pi]$$

$$\Delta f_i(t)_{max} = 12387.32\,\text{Hz}$$

$$\text{Hence, } \beta = \frac{12387.32}{1000}$$

$$\therefore \beta = 12.387 \approx 12$$

**65. Ans: (d)**

**Sol:** N = 5

$f_m = 100Hz$

$f_q = 200Hz$

$f_s$ = 50% higher than $f_q = 1.5\ f_q$

$\therefore f_s = 200 \times 1.5 = 300$ samples/sec

$r_b = [Nm + a]f_s$

$Nm = 5 \times 8 = 40$ bits

$$a = \frac{1.25}{100} \times 40 = \frac{5}{400} \times 40 = 0.5$$

$\therefore r_b = (40 + 0.5)300$

$r_b = 12150$ bps

**66. Ans: (d)**

**Sol:** $$\mu = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$$

$$= \frac{5-1}{5+1} = \frac{4}{6} = \frac{2}{3}$$

**67. Ans:(b)**

**Sol:** Transmission Bandwidth = $\frac{r_b}{2}(1+\alpha)$

[When Nyquist criterion pulses are used]

$$4\times10^3 = \frac{6\times10^3}{2}[1+\alpha] \Rightarrow 1 + \alpha = \frac{4}{3}$$

$$\therefore \alpha = \frac{4}{3} - 1 = \frac{1}{3} = 0.33$$

**68. Ans: (b)**

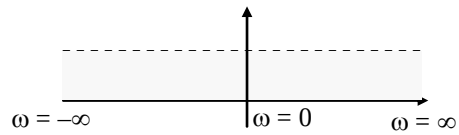
**Sol:** RST instruction is equivalent to 1-byte call instruction, however these software instructions used in a program to transfer program execution to one of the eight locations.

| | |
|---|---|
| RST0 | 0000 H |
| RST1 | 0008 H |
| RST2 | 0010 H |
| . | . |
| . | . |
| RST6 | 0030 H |
| RST7 | 0038 H |

**69. Ans: (d)**

**Sol:** **Statement (I):** If impulse is applied to second order system, it oscillates with its natural frequency, only if the poles lie on the imaginary axis.

**Statement (II):** Impulse consists of infinite frequency components, whose spectrum is shown in figure below.




**70. Ans: (d)**

**Sol:** Given C.E is

$4s^2 + 6s + 1 = 0$ …….. (1)

Standard form of characteristic equation is,

$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0$ ……. (2)

Compare eq. (1) and (2), then we get

$\omega_n = 0.5$ rad/sec and $\zeta = 1.5$

System is over damped ($\zeta > 1$)

**71. Ans: (a)**

**Sol:** $\text{CLTF} = \dfrac{G(s)}{1+G(s)H(s)}$

$CE = 1 + G(s)H(s) = 0$

For system to be stable roots (zeros) of characteristic equation must lie on left half of s-plane.

Poles of CLTF is nothing but zeros of characteristic equation.

**72. Ans: (b)**

**Sol:** Both the statements are correct but statement (II) is not the reason for Statement (I).

**73. Ans: (a)**

**Sol:** In a BJT, the majority of the stored charge is in the form of minority carriers which are diffusing across the device in forward operation. Whereas in FET current is only due to majority carriers. So there is no minority stored charge in FET.

Both the statements are true and statement (II) is correct reason for statement (II).

**74. Ans: (c)**

**Sol:** As reverse voltage changes minority carriers will not change, they change only due to temperature. So, statement (II) is false.

$I_o$ is not depends on reverse biased voltage.

So $\dfrac{dI_0}{dV} = 0$ .statement(I) is true.

**75. Ans: (c)**

**Sol:** **Statement (I):** is true because $(0100\ 0111\ 1000\ 1001)_2$, 16 bit can be stored as $(4789)_{16}$ in hexadecimal.

**Statement (II):** is False, since four times of binary number is 8 not 16.

ACE Engineering Academy
Since 1995

# ACE
## Engineering Academy
Leading Institute for ESE/GATE/PSUs

23 Years of Excellence

# CONGRATULATIONS TO OUR
# ESE - 2018 TOP RANKERS

AIR 1 —  SHASHANK E&T

AIR 1 —  CHIRAG JHA EE

AIR 1 —  VINAY PRAKASH CE

AIR 1 —  AMAN JAIN ME

AIR 2 —  CHERUKURI SAIDEEP E&T

AIR 2 —  SHADAB AHAMAD EE

AIR 2 —  PUNIT SINGH CE

AIR 2 —  CHIRAG SINGLA ME

AIR 3 —  RAMESH KAMULLA E&T

AIR 3 —  SRIJAN VARMA EE

AIR 3 —  PRAVEEN KUMAR CE

AIR 3 —  MAYUR PATIL ME

AIR 4 —  JAPJIT SINGH E&T

AIR 4 —  ANKIT GARG EE

AIR 4 —  AMIT KUMAR ME

AIR 5 —  NARENDRA KUMAR E&T

AIR 5 —  KARTHIK KOTTURU EE

AIR 5 —  RISHABH DUTT CE

AIR 5 —  VITTHAL PANDEY ME

AIR 6 —  KUMUD JINDAL E&T

AIR 6 —  RATIPALLI NAGESWAR EE

AIR 7 —  KARTIKEYA DUTTA E&T

AIR 7 —  TEKCHAND DESHWAL EE

AIR 7 —  ROHIT KUMAR CE

AIR 8 —  SURYASH GAUTAM E&T

AIR 8 —  RAVI TEJA MANNE EE

AIR 8 —  VIJAYA NANDAN CE

AIR 8 —  ROHIT BANSAL ME

AIR 9 —  SHANAVAS CP E&T

AIR 9 —  SOUVIK DEB ROY EE

AIR 9 —  ROOPESH MITTAL CE

AIR 10 —  PRATHAMESH E&T

AIR 10 —  MILAN KRISHNA EE

AIR 10 —  SRICHAND POONIYA CE

| TOTAL SELECTIONS in Top 10 | 34 |
|---|---|

| | TOP 10 |
|---|---|
| E&T | 10 |
| EE | 10 |
| CE | 8 |
| ME | 6 |

and many more...

www.aceenggacademy.com