ACE Engineering Academy

Head Office : Sree Sindhi Guru Sangat Sabha Association, # 4-1-1236/1/A, King Koti, Abids, Hyderabad – 500001.

Ph: 040-23234418, 040-23234419, 040-23234420, 040 - 24750437

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ESE- 2019 (Prelims) - Offline Test Series Test-13

ELECTRONICS & TELECOMMUNICATION ENGINEERING

SUBJECT: CONTROL SYSTEMS, ANALOG ELECTRONICS AND DIGITAL ELECTRONICS & MICRO-PROCESSORS

SOLUTIONS

01. Ans: (a)

Sol: Number of forward paths = 4

$Rx_1x_2x_3x_4C$

$Rx_1x_3x_4C$

$Rx_1x_2x_4C$

$Rx_1x_3x_2x_4C$

Number of loops = 5

$x_1x_2x_4x_1$

$x_2x_3x_2$

$x_1x_3x_4x_1$

x1x2 x_3x4x1

$x_1x_3x_2x_4x_1$

02. Ans: (c)

Sol: $S_K^T = \frac{\partial T}{\partial K}\frac{K}{T}$

$$= \frac{\partial}{\partial K}\left(\frac{1+3K}{1+2K}\right)\frac{K}{\left(\frac{1+3K}{1+2K}\right)}$$

$$= \left[\frac{(1+2K)3-(1+3K)2}{(1+2K)^2}\right]\frac{K(1+2K)}{1+3K}$$

$$= \frac{K}{(1+3K)(1+2K)}$$

$$= \frac{K}{1+5K+6K^2}$$

Substitute K = 1

$$S_K^T = \frac{1}{12}$$

03. Ans: (d)

Sol: $c(t) = L^{-1}[R(s).G_2(s)]$

$= L^{-1}\left[\frac{1}{s}.\frac{1}{s+2}\right]$

$= 0.5\,(1 - e^{-2t})\,u(t)$

04. Ans: (c)

Sol: $CE = s^4 + 2s^2 + 3 = 0$

s^4	1	2	3
s^3	0(4)	0(4)	0
s^2	1	3	
s^1	–8	0	
s^0	3		

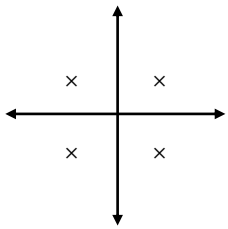
Given equation is AE, $\frac{dAE}{ds} = 4s^3 + 4s = 0$

Number of sign changes below the AE = 2

Number of RHP = Number of LHP = 2

Number of $j\omega P = 0$

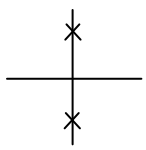
The four poles are located in quadrate as shown below



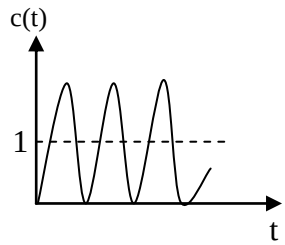
05. Ans: (a)

Sol: **Location of poles** **Unit step response**

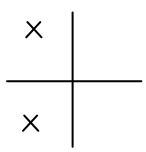
(A)



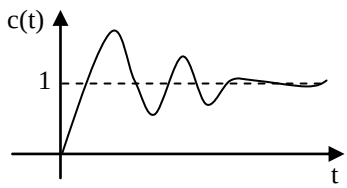
(4)



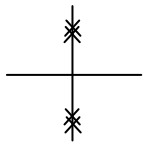
(B)



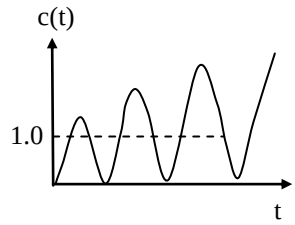
(1)



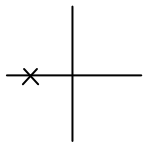
(C)



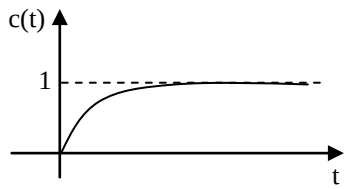
(2)



(D)



(3)



06. Ans: (c)

Sol: $$\frac{V_o(s)}{V_i(s)}=\frac{\left[\frac{1}{Cs}\right]\left[\frac{1}{Cs}\right]}{R\left[R+\frac{1}{Cs}+\frac{1}{Cs}\right]+\frac{1}{Cs}\left[R+\frac{1}{Cs}\right]}$$

Substitute R = 1Ω, C = 1F

$$\frac{V_o(s)}{V_i(s)}=\frac{1}{s^2+3s+1}$$

07. Ans: (c)

Sol: C(s) = TF×R(s)

$$R(s)=L[\cos t]=\frac{s}{s^2+1}$$

$$C(s)=\frac{1}{s^2}\cdot\frac{s}{s^2+1}=\frac{1}{s(s^2+1)}=\frac{1}{s}+\frac{-s}{s^2+1}$$

$$c(t)=L^{-1}[C(s)]=1-\cos t$$

08. Ans: (d)

Sol: Noise transfer function $$\frac{C(s)}{N(s)}=\frac{G_1}{1-(-2G_1G_2H)}$$

$$=\frac{G_1}{2G_2G_1H+1}$$

09. Ans: (b)

Sol: From option (b)

$\omega=0.....\angle\phi=-270°$

$\omega=\infty.....\angle\phi=-180°$

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10. Ans: (b)

Sol: $\left|\frac{k}{s^2}\right|_{\omega=10} = 1$

$\frac{k}{\omega^2} = 1$

$k = \omega^2 = 10^2$

$\therefore K_a = k = 100$

11. Ans: (a)

Sol: The number of loops = 4

Loop gains = 1, 1, 1, –1

$\therefore$ Sum of individual loop gains = 1 + 1 + 1 – 1 = 2

12. Ans: (b)

Sol: $PM = 180° + \angle \frac{j\omega + 1}{(j\omega)^2\sqrt{2}}\Big|_{\omega=\omega_{gc}}$

$\left|\frac{j\omega_{gc} + 1}{(j\omega_{gc})^2\sqrt{2}}\right| = \frac{\sqrt{\omega_{gc}^{\ 2} + 1}}{\omega_{gc}^2\sqrt{2}} = 1$

$\omega_{gc} = 1 \text{rad/sec}$

$\therefore PM = 180° + \tan^{-1}\omega_{gc} - 180°$

$PM = 45°$

13. Ans: (c)

Sol: For region 1 N = –1

For region 2 N = –2

For region 3 N = 0

Given,

P = 0, Z = 0

$\therefore N = P - Z = 0$

Only if (–1, j0) lies in region (3) N is zero

14. Ans: (a)

Sol: A derivative controller

$\rightarrow$ improves the stability of the system

$\rightarrow$ improves phase margin

$\rightarrow$ decreases over shoot

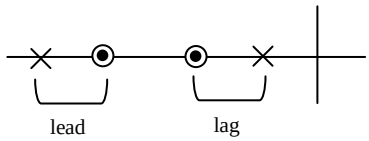
$\rightarrow$ decreases settling time

15. Ans: (b)

Sol: Transfer function of lag-lead compensator is

$G_c(s) = \frac{(s + Z_1)(s + Z_2)}{(s + P_1)(s + P_2)}$ where $P_1 < Z_1 < Z_2 < P_2$

Pole zero plot of lag-lead compensator



16. Ans: (b)

Sol: $k_p = \lim_{s\to 0} G(s) = \infty$

$k_v = \lim_{s\to 0} sG(s) = \infty$

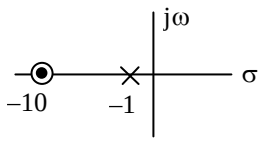
$k_a = \lim_{s\to 0} s^2G(s) = 10$

Error due to $1 + t + \frac{t^2}{2} = \frac{1}{1+k_p} + \frac{1}{k_v} + \frac{1}{k_a} = 0.1$

17. Ans: (b)

Sol: Let $G_c(s) = \frac{1+s/10}{1+s/1}$

Pole zero plot of lag compensator



18. Ans: (c)

Sol: Given positive feedback system

$\therefore$ Characteristic equation $1 - G(s)H(s) = 0$

$1 - \frac{k}{s-6} = 0$

$s - 6 - k = 0$

$s - (k + 6) = 0$

$k + 6 < 0$

$k < -6$

19. Ans: (c)

Sol: $G(s)\,H(s) = \frac{k}{s(s+1)(s+2)}$

$CE = 1 + G(s)H(s) = 0$

$s(s+1)(s+2) + k = 0$

$s^3 + 3s^2 + 2s + k = 0$

s^3	1	2
s^2	3	k
s^1	$\frac{6-k}{3}$	0
s^0	k	

$k_{marginal} = 6$

$\therefore$ The value of k at point A = 6

20. Ans: (b)

Sol: Every branch of the RLD starts at a pole (k = 0), and terminates at a zero (k = ∞) of the OLTF G(s)H(s).

On the real axis to the right side of any section, if the sum of total no. of open loop poles and zeros are odd, RLD exists in that section.

21. Ans: (d)

Sol: $\frac{C(s)}{R(s)} = T(s) = \frac{(s+2)e^{-s}}{(s^2+4)}$

Impulse response = L^{-1} (T(s))

$T(s) = \frac{se^{-s}}{s^2+4} + \frac{2e^{-s}}{s^2+4}$

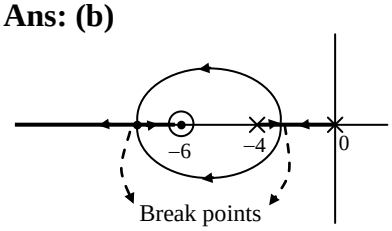
IR = L^{-1} (T(s))

$IR = L^{-1}\left[\frac{se^{-s}}{s^2+4}\right] + L^{-1}\left[\frac{2e^{-s}}{s^2+4}\right]$

IR = cos 2(t–1) + sin 2(t–1)

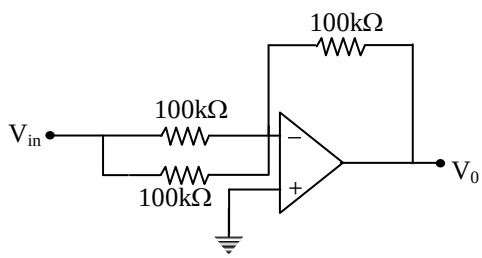
22. Ans: (b)

Sol:



23. Ans: (c)

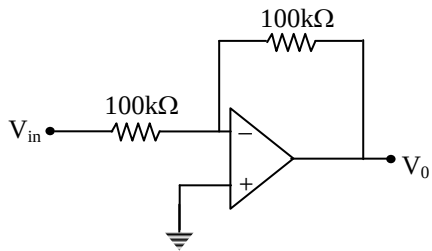
Sol: When the switch (S/W) is on:



$$V_0 = -\frac{R_f}{R} = -\frac{100\,k}{100\,k\,//\,100\,k} \times V_{in}$$

$$\frac{V_0}{V_{in}} = -2 \Rightarrow X = -2$$

When the switch is OFF:



$$\frac{V_0}{V_{in}} = \frac{-100k}{100k} = -1 \Rightarrow Y = -1$$

$X = -2, Y = -1$

$X = -1 - 1$

$X = Y - 1$

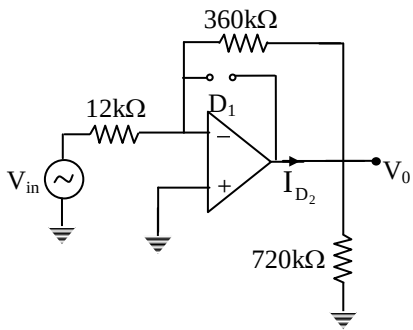
24. Ans: (c)

Sol: If the emitter bypass capacitor in a common emitter amplifier is removed,
i) The input resistance of the amplifier will be increased
ii) The voltage gain of the amplifier will be decreased.

25. Ans: (c)

Sol: During positive half-cycle of input voltage,
$D_1 \rightarrow$ ON
$D_2 \rightarrow$ OFF $\Rightarrow I_{D_2} = 0$

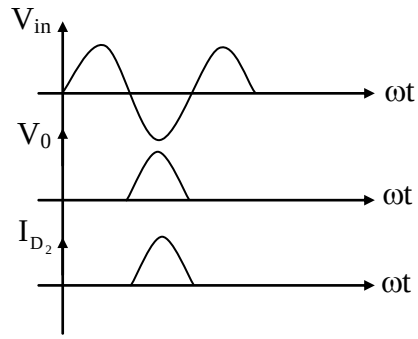
During negative half-cycle of input voltage,
$D_1 \rightarrow$ OFF
$D_2 \rightarrow$ ON



$V_0 = -30V_{in}$ and $V_{in} = -2\sin\omega t$

$\therefore V_0 = 60\sin\omega t$

The output voltage waveforms are shown below

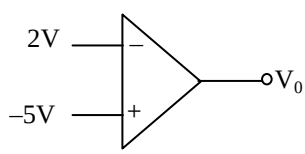


$$I_{D2} = \frac{V_0}{720k} + \frac{V_0}{360k} = \frac{V_0}{240k} = 0.25\sin\omega t \text{ mA when } V_{in} < 0$$

RMS value of $I_{D2} = \frac{0.25}{2} = 0.125\text{mA}$

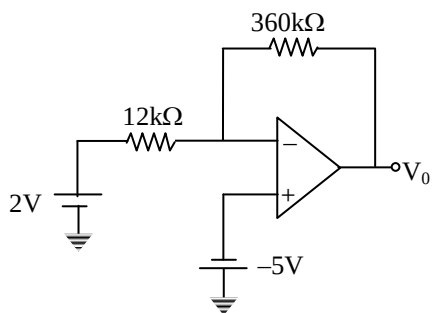
26. Ans: (c)

Sol: Open loop configuration:



$V_0 = (-5 - 2)\, A_0 \Rightarrow -Ve$

$\therefore D_1 \rightarrow$ OFF; D_2 is ON



$V_0 = -215$ V

$|V_0| \geq |-12| \quad \Rightarrow \quad V_0 = -12$ V

27. Ans: (c)

Sol:

(i) For cut-off region:

$V_{SG} < |V_{tp}|$

$V_S - V_G < 0.5$

$-V_G < 0.5 - 3$

$V_G > 2.5V$

(ii) For triode region:

$V_{SD} < V_{SG} - |V_{tp}|$

$V_S - V_D < V_S - V_G - 0.5$

$3 - 1 < 3 - V_G - 0.5$

$V_G < 0.5V$

(iii) For saturation region:

$V_{SD} \geq V_{SG} - |V_{tp}|$

$3 - 1 \geq 3 - V_G - 0.5$

$V_G \geq 0.5V$

28. Ans: (b)

Sol: $-V_{D2} + V_{D1} + V = 0$

$V = V_{D2} - V_{D1} = 50mV$

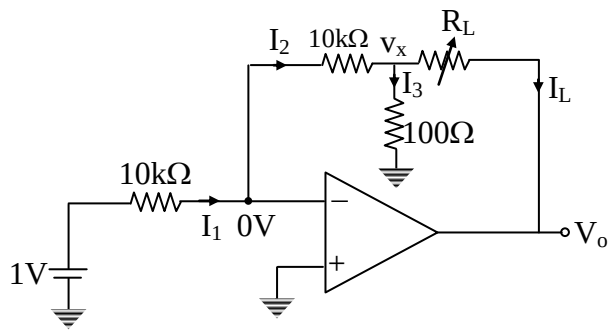
$10mV = I_1 + I_2$

$$\frac{I_2}{I_1} = \frac{I_s e^{\frac{V_{D2}}{V_T}}}{I_s e^{\frac{V_{D1}}{V_T}}} = e^{\frac{V_{D2}-V_{D1}}{V_T}}$$

$$\frac{I_2}{I_1} = e^{\frac{50mV}{25mV}} = e^2$$

29. Ans: (c)

Sol:



$$I_1 = \frac{1}{10k} = 0.1mA$$

$I_2 = I_1 = 0.1mA$

$(10k\ I_2) + (100\ I_3) = 0$

$$I_3 = \frac{-10k \times 0.1m}{100} = -10mA$$

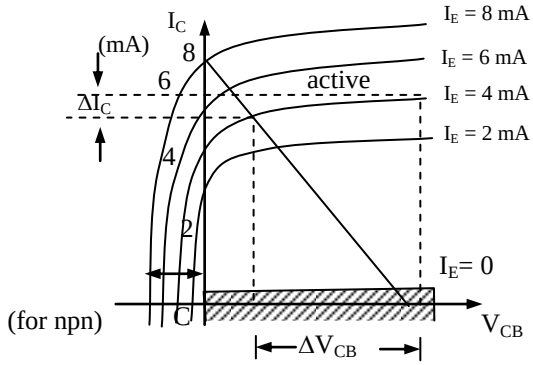
$V_x = -100 \times 10m$

$V_x = -1V;$

$I_L = I_2 - I_3$
$= 10.1mA$
$V_0 = V_x - I_L R_L$
$V_0 = -1 - 10.1m\ R_L$
When $R_L = 100\Omega$
$\rightarrow$ $V_{0max} = -1 - (10.1\times10^{-3}\times100)$
$= -2.01V$
When $R_L = 1k\Omega$
$\rightarrow$ $V_{0min} = -1 - (10.1\times10^{-3}\times10^{3})$
$= -11.1V$
$-11.1V < V_0 < -2.01V$

30. Ans: (c)

Sol: **Output Characteristics: I_C vs $V_{CB}|I_E$**



Saturation Region:

- Saturation region is the region left side to $V_{CB} = 0$ line.
- In saturation region, emitter and collector junction are in forward bias.
- In saturation region, collector current increases exponentially.
- It can be used as ON switch in saturation region.

31. Ans: (c)

Sol: The emitter capacitance (C_E)is increases the gain $\left(\frac{V_0}{V_s}\right)$ and input resistance (R_{in}) decreases for AC signals.

32. Ans: (c)

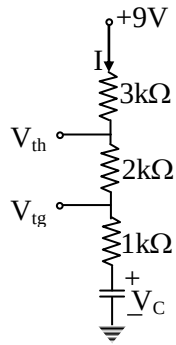
Sol: A 555 timer change the state when threshold voltage, V_{th} is just greater than $\frac{2V_{CC}}{3}$ volts and trigger voltage, V_{tg} is just below the $\frac{V_{CC}}{3}$ volts.

$V_{th} = \frac{2}{3}\times 9 = 6V$

$I = \frac{9-6}{3k} = 1mA$

Apply KVL:

$-6 + 2 + 1 + V_C = 0 \Rightarrow V_C = 3V$



$V_{tg} = \frac{1}{3} \times 9 = 3V$

$I = \frac{9-3}{5k} = \frac{6}{5} mA$

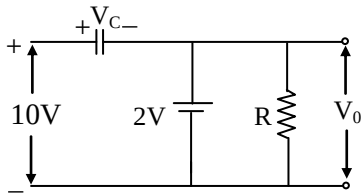
$V_C = 1.8V$

Therefore, the range of the voltage across the capacitor, V_c is 1.8V to 3V

33. Ans: (c)

Sol: When $V_i = +10V$, diode is forward biased

$\therefore V_0 = 2V$

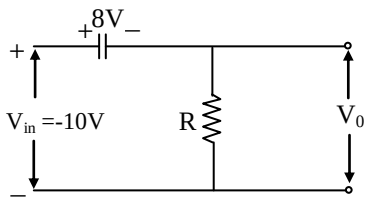


$-10 - V_C - V_0 = 0$

$10 - V_C - 2 = 0$

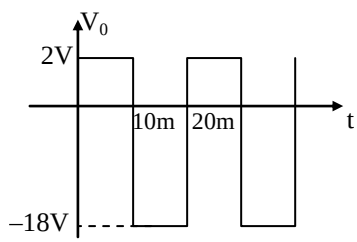
$V_C = +8V$

When $V_{in} = -10V$, diode is reverse biased.



$-10 - 8 = V_0 \Rightarrow V_0 = -18V$

The output wave form:



Average output voltage,

$V_0 = \frac{2 \times 10m - 18 \times 10m}{20m} = -8V$

34. Ans: (c)

Sol: In E-MOSFET

$V_{GS} = 0$ then $I_D = 0$

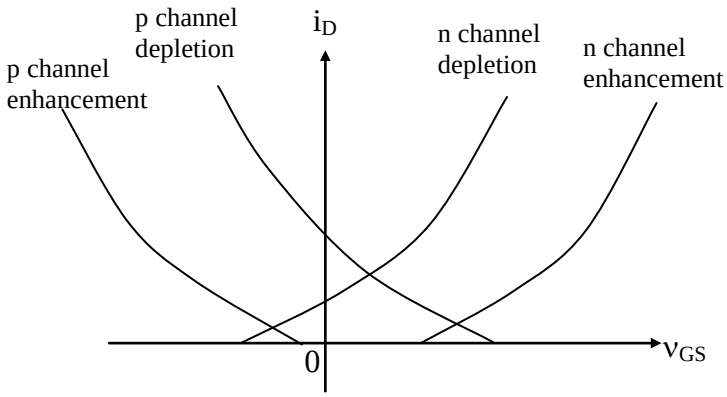
If $+V_{GS}$ increases then 'I_D' also Increases

35. Ans: (c)

Sol: The phase of loop gain should be zero. So statement(ii) is wrong.

36. Ans: (c)

Sol:



$\therefore$ P- III, Q-II, R-IV, S-I

37. Ans: (c)

Sol: Overall voltage gain = product of individual voltage gains = 25×10×4 = 1000

Overall gain in dB = $20 \log_{10} 1000 = 60$dB

38. Ans: (d)

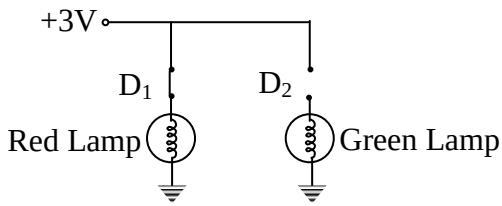
Sol: $I_D = \dfrac{2.5-1.8}{R}$

$0.5\text{mA} = \dfrac{0.7\text{V}}{R}$

$R = \dfrac{0.7}{0.5\text{m}} = 1.4\text{k}\Omega$

39. Ans: (b)

Sol: For $V_i = 3$V, D_1 is in forward bias, D_2 is in reverse bias

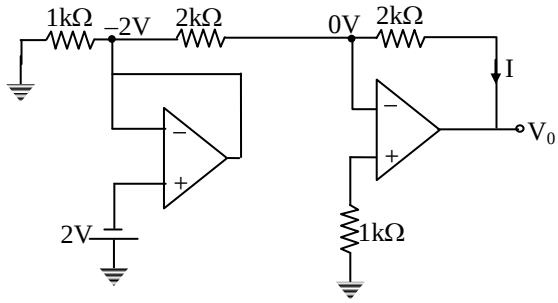


$\therefore$ RED lamp gets ON

GREEN lamp gets OFF

40. Ans: (c)

Sol: By open-loop comparator, D_1 is ON and D_2 is OFF



$$\frac{0+2}{2k}+\frac{0-V_0}{2k}=0$$

$$V_0 = 2V$$

The current through resistor, $I=\frac{-2}{2k}=-1mA$

41. Ans: (a)

Sol: $$f_L'=\frac{f_L}{\sqrt{2^{\frac{1}{n}}-1}}$$

$$f_L'=\frac{20}{\sqrt{2^{1/3}-1}} = 39.229 \text{ Hz}$$

42. Ans: (a)

Sol: 1. The Leakage current I_{CB0} doubles for every 10^0C rise in temperature.
2. Base emitter voltage V_{BE} decreases by 2.5 mV for every 1^0C rise in temperature.
3. As temperature increases I_c increases so power dissipation at the junction increases.

43. Ans: (a)

Sol: $I_c = \beta I_B + I_{CE0}$
$= \beta I_B + (\beta+1) I_{CB0}$
$= 100\ (10\mu A) + 101\ (100\ nA)$
$= 1\ mA + 0.0101mA$
$= 1.0101\ mA$

44. Ans: (c)

Sol: $$V_{3k}=15.\frac{3}{2+3}$$
$= 9V$

$V_{3k} < Vz$ Hence zener diode is O.C

Hence

$$I_L=\frac{15}{2K+3K}=3mA$$

45. Ans: (b)

Sol: 1. Crystal oscillators were used whenever the greater stability of oscillations are required
2. RC oscillators are low frequency oscillators
3. LC oscillators are high frequency oscillators
4. In Hartley oscillator mutual inductance between two feedback inductors will effects the frequency of oscillation

46. Ans: (b)

Sol: If $V_{in} > V_{out}$ set next bit
If $V_{in} < V_{out}$ set bit is going to reset and will set next bit
Here given that,
Analog input (V_{in}) = 6.2V
Digital output is greater than 6.2V so reset the last set bit and set the next bit.
Given digital input is equal to 11010000
$\therefore$ next value of SAR is 11001000

47. Ans: (c)

Sol: The maximum number of Boolean functions with
'n' variables = 2^{2^n}
For '5' variables = 2^{2^5}
$= 2^{32}$
= 4294967296

48. Ans: (b)

Sol: 1) Without using any additional logic gates , we cannot implement all Boolean functions using decoder.
2) Any function can be implemented using suitable MUX.
3) MUX is producing only one output, it cannot be used for multiple output function.

49. Ans: (b)

Sol: $f(A,B,C,D) = \prod M(0,4,5,7,12,15)$
$= \Sigma m\ (1,2,3,6,8,9,10,11,13,14)$

A B / S_1 S_0	I_0 0 0	I_1 0 1	I_2 1 0	I_3 1 1
$\overline{C}\overline{D}$ (00)	0	4	⑧	12
$\overline{C}D$ (01)	①	5	⑨	⑬
$C\overline{D}$ (10)	②	⑥	⑩	⑭
CD (11)	③	7	⑪	15
	C+D	$C\overline{D}$	1	C⊕D

$I_0 = C + D$
$I_1 = C\overline{D}$
$I_2 = 1$
$I_3 = C \oplus D$

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50. Ans: (d)

Sol: $f(A, B, C, D) = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}BCD + A\overline{B}CD + ABCD$

$= \Sigma m(0, 1, 2, 3, 7, 11, 15)$

AB \ CD	00	01	11	10
00	1	1	1	1
01			1	
11			1	
10			1	

The simplified form of f(A, B, C, D) = $\overline{A}\,\overline{B} + CD$

51. Ans: (c)

Sol: $(63)_{16} + (37)_{16} = (9A)_{16}$

$\therefore Y = 9A\ H$

52. Ans: (b)

Sol: It is up counter

All the flip flops are clearing when $Q_2\ Q_1 = 11$

0 0 0
0 0 1
0 1 0
0 1 1
1 0 0 $\Rightarrow$ 0 0 0

As it is asynchronous counter 100 state is overwriting with 000.

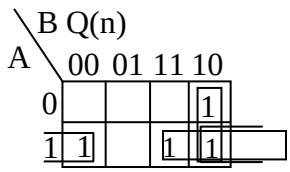
So it is counting only 4 states

53. Ans: (a)

Sol:

A	B	Q(n+1)
0	0	0
0	1	$\overline{Q(n)}$
1	0	$\overline{Q(n)}$
1	1	1

	A	B	Q(n)	Q(n+1)
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1



$$Q(n+1) = A\overline{Q(n)} + B\overline{Q(n)} + AB$$

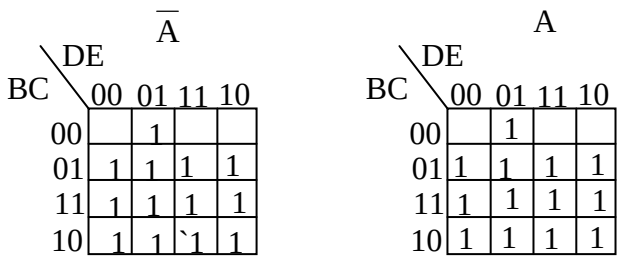
54. Ans: (d)

Sol: The 10's complement of decimal number = 9's complement + 1

$$\begin{array}{rr} & 9999\,.\,99999 \\ (-) & 6091\,.\,20100 \\ \hline 9\text{'s complement} \Rightarrow & 3908\,.\,79899 \\ (+) & \qquad\qquad 1 \\ \hline 10\text{'s complement} \Rightarrow & 3908\,.\,79900 \end{array}$$

55. Ans: (c)

Sol:



Total number of minterms = 26

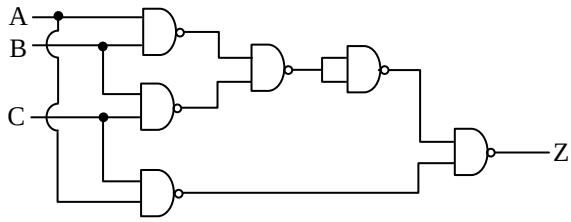
56. Ans: (c)

Sol: $f = AB + BC + AC$

$$= \overline{\overline{AB + BC + AC}}$$

$$= \overline{\overline{AB}.\overline{BC}.\overline{AC}}$$

$$= \overline{\overline{AB}.\overline{BC}}.\overline{\overline{AC}}$$



The function requires minimum 6 number of NAND gates to be realized.

57. Ans: (c)

Sol: ECL logic family has

(1) Very high switching speed

(2) High power dissipation

(3)

Voltage Level	State	Boolean Logic
–0.8V	HIGH	Logic '1'
–1.8V	LOW	Logic '0'

ECL logic family uses negative voltage levels for both logic 1 and 0.

(4) Fan-out capability is high

58. Ans: (d)

Sol: In fourth generation embedded system, the system on chip(SOC) is used.

59. Ans: (a)

Sol: Given that rotor is at "C" initially

Input (xy)	Rotor Position
	C
00	C
01	D
10	C
10	B
11	B
00	B
10	A
11	A

Therefore position of rotor after the inputs in given sequence is 'A' .

60. Ans: (c)

Sol: 1) Registers are made of edge triggered flops where as latches are made from level triggered flip flops.

2) Latch employs cross coupled feed back connections.

3) Noise immunity is the amount of noise which can be applied at the input of the gate without causing the gate to change state.

4) Propagation delay is the time required for a gate to change its state.

61. Ans: (c)

Sol: S_1: Flash ADC is fastest ADC.
S_2: The most widely used ADC in multimeter is Successive approximation ADC.
S_3: The conversion time for Successive approximation ADC depends only on number of output bits. It doesn't depends on applied input voltage.
S_4: In dual slope ADC integrator is used.

62. Ans: (d)

Sol: CMOS logic family is having the given two merits, Hence it became familiar in most of the real time applications today.

63. Ans: (d)

Sol:
```
MVI   A, 06H ; [A] = 06H = 00000110
RLC          ; [A] = 00001100 = 0CH
MOV   B, A   ; [B] = 0CH = 00001100
RLC          ; [A] = 00011000
RLC          ; [A] = 00110000 = 30H
ADD   B      [A] = [A]+[B] = 30H + 0CH = 3CH
HLT
```

64. Ans: (c)

Sol: The 8051 requires an external oscillator circuit. The oscillator circuit usually runs around 12MHz. Each machine cycle in the 8051 is 12 clock cycles, giving an effective cycle rate at 1MHz to 3.33 MHz.
One Machine cycle has 6 states. One state is 2T-states.
$\therefore$ One machine cycle is 12T-states.

65. Ans: (c)

Sol: Interrupt vector table on 8086 is a vector that consists of 256 total interrupts placed at first 1kB of memory from 0000H to 03FFH.

66. Ans: (b)

Sol: Segmentation is a technique for allocating memory in chunks of varying and meaningful sizes instead of one arbitray page size i.e., segmentation splits the memory into unequal units.
Therefore statement (3) is wrong

67. Ans: (b)

Sol:

(A) XTHL: Exchanges the contents of H and L registers with top of stack.
It takes 5 machine cycles = 16T states

(B) PUSH B: The contents of the register pair designated in the operand are copied onto the stack in the following sequence. The stack pointer register is decremented and the contents of the high order register (B) are copied into the location.
The stack pointer register is decremented again and the contents of the low-order register (C) are copied to that location.
3 Machine cycles = 12 T-states

(C) HLT: Halt and enter into wait state
It takes 5 T-states.

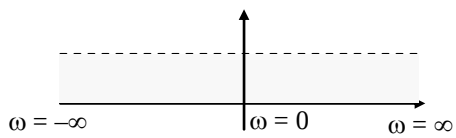
(D) XCHG: The contents of the register H are exchanged with the contents of register D, and the contents of register L are exchanged with the contents of register E.
1-Fetch machine cycle = 4T states

68. Ans: (d)

Sol: AAD stands for "ASCII Adjust before Division".
This instruction adjusts two unpacked BCD digits (Least significant digit in AL register and the most significant digit in AH register) so that a division operation performed on the result will yield a correct unpacked BCD value.
AAD instruction useful only when it precedes a DIV instruction.

69. Ans: (d)

Sol: **Statement (I):** If impulse is applied to second order system, it oscillates with its natural frequency, only if the poles lie on the imaginary axis.
Statement (II): Impulse consists of infinite frequency components, whose spectrum is shown in figure below.



70. Ans: (d)

Sol: Given C.E is
$4s^2 + 6s + 1 = 0 \quad \rightarrow (1)$
Standard form of characteristic equation is,
$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0 \rightarrow (2)$
Compare eq(1) and (2),then we get
$\omega_n = 0.5$ rad/sec and $\zeta = 1.5$
System is over damped ($\zeta > 1$)

71. Ans: (a)

Sol: $\text{CLTF} = \dfrac{G(s)}{1+G(s)H(s)}$
$CE = 1 + G(s)H(s) = 0$

For system to be stable roots (zeros) of characteristic equation must lie on left half of s-plane.

Poles of CLTF is nothing but zeros of characteristic equation.

72. Ans: (b)

Sol: Both the statements are correct but statement (II) is not the correct explanation for Statement (I).

73. Ans: (a)

Sol: In a BJT, the majority of the stored charge is in the form of minority carriers which are diffusing across the device in forward operation. Whereas in FET current is only due to majority carriers. So there is no minority stored charge in FET.
Both the statements are true and statement (II) is correct explanation for statement (II).

74. Ans: (d)

Sol: DRAM stores charge in the form of charge. Each memory cell in DRAM is made of transistor and capacitor. The data will be stored in capacitor. So, DRAM must be refreshed regularly since capacitor loose charge due to leakage.
SRAM is faster than DRAM since it doesn't have refreshing circuit.

75. Ans: (c)

Sol: **Statement (I)** is true because $(0100\ 0111\ 1000\ 1001)_2$, 16 bit can be stored as $(4789)_{16}$ in hexadecimal.
Statement (II) is False, since four times of binary number is 8 not 16.

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