TEST ID: 201

ACE Engineering Academy

Head Office : Sree Sindhi Guru Sangat Sabha Association, # 4-1-1236/1/A, King Koti, Abids, Hyderabad – 500001.

Ph: 040-23234418, 040-23234419, 040-23234420, 040 - 24750437

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ESE- 2019 (Prelims) - Offline Test Series Test-1

ELECTRICAL ENGINEERING

SUBJECT: ANALOG, DIGITAL ELECTRONICS AND BASIC ELECTRONICS ENGINEERING

SOLUTIONS

01. Ans: (d)

Sol:

1. With increase in the temperature zener break down voltage reduces
2. The Avalanche breakdown voltage has positive temperature coefficient
3. Zener breakdown occurs due to large electric field across reverse biased junction
4. Avalanche break down occurs in lightly doped junctions

02. Ans: (b)

Sol: $C_D = \frac{\tau I}{\eta V_T} = \frac{1n \times 1m}{25m}$

$= \frac{1n}{25}$

$= \frac{1000PF}{25}$

$= 40PF$

Derivation for diffusion capacitance:

$C_D = \frac{dQ}{dV_D}$

$Q = \tau I_s\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$

$\frac{dQ}{dV_D} = \frac{\tau I_s e^{\frac{V_D}{\eta V_T}}}{\eta v_T}$

$= \frac{\tau I}{\eta v_T}$

03. Ans: (b)

Sol: $I_D = I_s\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$

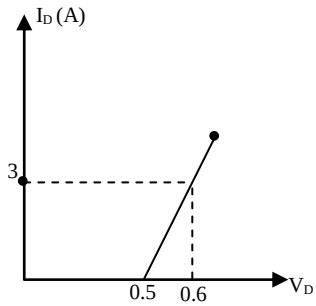
$\frac{dI_D}{\partial V_D} = \frac{I_s e^{\frac{V_D}{\eta V_T}}}{\eta v_T}$

$\cong \frac{I_D}{\eta V_T}$

$r_{dynamic} = \frac{\partial V_D}{\partial I_D} = \frac{\eta V_T}{I_D} = \frac{26mv}{20m} = 1.3\Omega$

04. Ans: (b)

Sol:



$$P_D = V_D I_D + I_D^2 r_{DC}$$

$$r_{DC} = \frac{V_D}{I_D} = \frac{0.6}{3}$$

$$= 0.2$$

$$P_D = 0.5\times 3 + (3)^2 \times 0.2$$

$$= 1.5 + 1.8$$

$$= 3.3\ W$$

05. Ans: (c)

Sol: $V_{3k} = 15.\frac{3}{2+3}$

$$= 9V$$

$V_3k < Vz$ Hence zener diode is O.C

Hence

$$I_L = \frac{15}{2k+3k} = 3mA$$

06. Ans: (d)

Sol: As V_{CB} increases

1. Recombination of the charge carriers with in the base decreases.
2. The concentration gradient of minority carriers increases with in the base.
3. C.E. current gain β increases.
4. CB current gain α increases.

07. Ans: (d)

Sol:

1. In the input characteristics of C.E. Configuration for same V_{BE} as V_{CE} increases, input current I_B decreases.
2. The input resistance of C.B. configuration is less compared to C.E.
3. Only voltage gains is high in C.B. configuration and current gain is approximately equal to 1.

08. Ans: (a)

Sol:

1. The Leakage current I_{CB0} increases
2. Base emitter voltage V_{BE} decreases.
3. Power dissipation increases

09. Ans: (a)

Sol: $$I_D = I_{Dss}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{-2I_{Dss}}{V_p}\left(1-\frac{V_{GS}}{V_p}\right)$$

$$= -2\times\frac{2mA}{-4}\left(1-\frac{-2}{-4}\right)$$

$$= 1m\left(1-\frac{1}{2}\right)$$

$$= 0.5\ m\text{℧}$$

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10. Ans: (a)

Sol: $I_c = \beta I_B + I_{CE0}$

$= \beta I_B + (\beta+1) I_{CB0}$

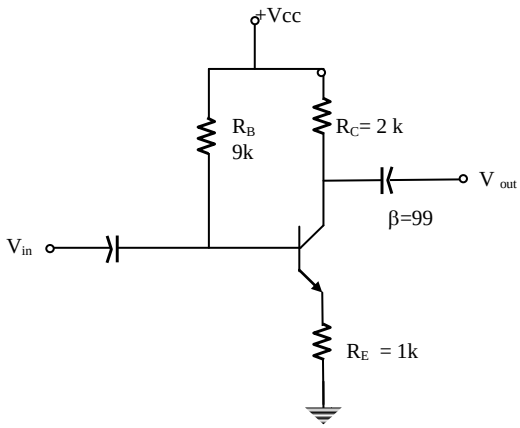
$= 100\ (10\mu A) + 101\ (100\ nA)$

$= 1mA + 0.0101mA$

$= 1.0101\ mA$

11. Ans: (b)

Sol:



$$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_E+R_B}}$$

$$= \frac{1+99}{1+99\left(\dfrac{1}{10}\right)}$$

$$= \frac{100}{10.9} = 9.17$$

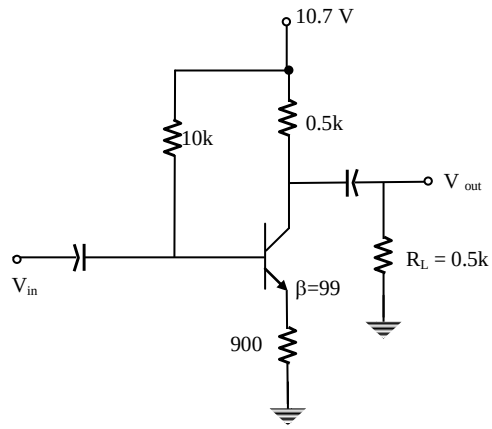
12. Ans: (a)

Sol: For thermal stability of the BJT amplifier, the rate at which heat released at the junction must be less than rated which heat is transfer to the atmosphere.

So, $\dfrac{\partial P_C}{\partial T_J} < \dfrac{1}{\theta_{JA}}$

13. Ans: (c)

Sol:



$10.7 = 10kI_B + (\beta+1)\ I_B\ (900) + 0.7$

$\beta = 99$

$10.7 = [\ 10k + 100\ (900)]\ I_B + 0.7$

$10 = (100k)\ I_B$

$$I_B = \frac{1}{10}mA$$

$= 0.1mA$

$I_E = (\beta+1)\ I_B$

$= (0.1)\ m\ (100)$

$= 10\ mA$

$$r_e = \frac{V_T}{I_E} = \frac{25m}{10m}$$

$= 2.5\Omega$

$h_{ie} = h_{fe} \times r_e$

$$A_V = \text{gain} = \frac{-h_{fe}}{h_{ie}}\left(R_C // R_L\right)$$

$$= -\frac{\left(R_C // R_L\right)}{r_e} = -\frac{0.5k // 0.5k}{2.5}$$

$$= -\frac{0.25k}{2.5}$$

$= -100$

14. Ans: (a)

Sol: $V_0 = -g_m [R_D \parallel R_L \parallel r_d]$

$r_d \approx \infty$

$= -2m [10\ k \parallel 10\ k]$

$= -2m [5k]$

$= -10$

15. Ans: (a)

Sol: $f_L' = \dfrac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}}$

$f_L' = \dfrac{20}{\sqrt{2^{1/3} - 1}} = 39.229$

16. Ans: (a)

Sol: From DC analysis

$V_B = \dfrac{11.4}{2} = 5.7\ V$

$V_B = V_{BE} + I_E R_E$

$5.7 = 0.7 + I_E\ 1k$

$5\ mA = I_E$

$r_e = \dfrac{V_T}{I_E} = \dfrac{25mV}{5mA} = 5\ \Omega$

Let $r_0 = \infty$

Voltage gain $= -\dfrac{r_0 \parallel R_c}{r_e} = \dfrac{1k}{5} = -200$

$C_i = C_{\omega i} + C_{be} + C_{bc} [1 - A_V]$

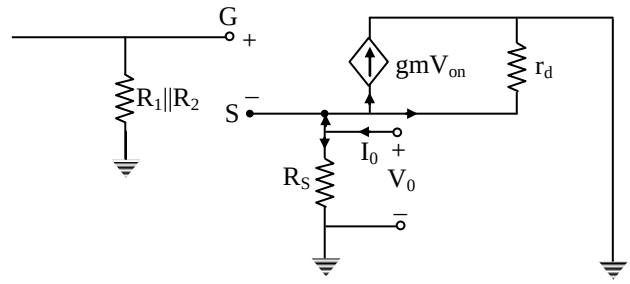
$= 1\ pF + 1\ pF + 0.1\ [1 + 200]pF$

$= 2\ pF + 201\ pF$

$= 22.1\ pF$

17. Ans: (b)

Sol: Equivalent circuit



$V_{GS} = -V_0$

$I_0 = \dfrac{V_0}{R_s} + \dfrac{V_0}{r_d} + g_m V_{GS}$

$= V_0 \left[\dfrac{1}{R_s} + \dfrac{1}{r_d} + g_m\right]$

$\dfrac{V_0}{I_0} = \dfrac{1}{\dfrac{1}{R_s} + \dfrac{1}{r_d} + \dfrac{1}{1/g_m}}$

$= R_s \parallel r_d \parallel 1/g_m$

$= 2k \parallel 1/1m$

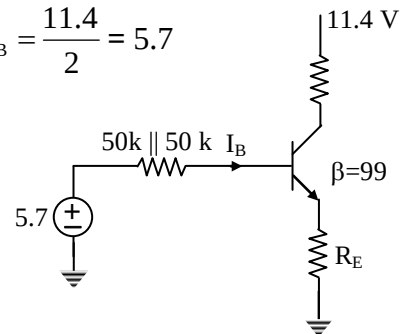
$= \dfrac{2 \times 1}{2+1} = \dfrac{2}{3}k$

$= 666.66\ \Omega$

18. Ans: (a)

Sol: DC analysis:

$V_B = \dfrac{11.4}{2} = 5.7$



$$I_B = \frac{5.7 - 0.7}{25k} = \frac{5}{25k} = 0.2 \text{ mA}$$

$$I_E = (1 + \beta)\, I_B = 100(0.2 \text{ mA})$$

$$= 20 \text{ mA}$$

$$r_e = \frac{V_E}{I_E} = \frac{25\text{mV}}{20\text{mA}} = 1.25\ \Omega$$

$$h_{ie} = \beta \times r_e = 1.25 \times 99 = 123.75$$

$$\text{Let } \omega_{Li} = \frac{1}{R_{in}.C_{in}}$$

$$R_{in} = R_1 \parallel R_2 \parallel h_{ie}$$

$$= 50 \text{ k} \parallel 50 \text{ k} \parallel 123.75$$

$$= 123$$

$$\omega_{Li} = \frac{1}{123 \times 100\mu} = 81 \text{ rad/sec}$$

19. Ans: (a)

Sol: $f_T = \dfrac{1}{2\pi r_e (C_{bc} + C_{be})}$

DC analysis:

$$I_B = \frac{10.7 - 0.7}{4k}$$

$$= \frac{10}{4k} = 2.5 \text{ mA}$$

$$r_e = \frac{V_I}{I_E} = \frac{25\text{mV}}{2.5\text{mA}} = 10\ \Omega$$

$$f_T = \frac{1}{2\pi(10)(2) \times 10^{-12}}$$

$$= \frac{1}{40\pi \times 10^{-12}}$$

$$= \frac{10^{12}}{40\pi} = 7.957 \text{ GHz}$$

20. Ans: (b)

Sol: $R_{if} = \dfrac{R_i}{1 + AB} = \dfrac{20}{1 + (10)(0.9)} = 2\ \Omega$

21. Ans: (a)

Sol: Here the feedback element is R_2 and the sampling signal is part of the output voltage V_0. Hence voltage sampling feedback element is connected in series with the input hence voltage mixing.

The given amplifier is voltage series amplifier.

22. Ans: (a)

Sol: $\beta = \dfrac{V_f}{V_0}$

$$= \frac{R_2}{R_1 + R_2} = \frac{10}{20} = \frac{1}{2} = 0.5$$

$$A_f = \frac{A}{1 + A\beta} = \frac{18}{1 + 18(0.5)} = 1.8$$

23. Ans: (b)

Sol: The given amplifier is current amplifier. By using feedback, input resistance decreases and output resistance increases.

24. Ans: (b)

Sol: $\omega_0 = \dfrac{1}{\sqrt{LC_{eq}}}$

$$C_{eq} = \frac{C_1.C_2}{C_1 + C_2} = \frac{900\text{p}}{100} = 9 \text{ pF}$$

$$= \frac{1}{\sqrt{1\mu 9p}}$$

$$= \frac{1}{\sqrt{9\times10^{-18}}}$$

$$= \frac{10^9}{3} \text{ rad/sec}$$

$$= 3.33 \times 10^8 \text{ rad/sec}$$

$$\beta = \frac{C_2}{C_1} = \frac{10}{90} = \frac{1}{9}$$

25. Ans: (b)

Sol:

1. Crystal oscillators were used whenever the greater stability of oscillations are required
2. RC oscillators are low frequency oscillators
3. LC oscillators are high frequency oscillators
4. In Hartley oscillator mutual inductance between two feedback inductors will effects the frequency of oscillation

26. Ans: (d)

Sol: (1) $f = \frac{1}{2\pi\sqrt{R_3R_4C_1C_2}}$

(2) $\frac{R_2}{R_1} = \frac{R_3}{R_4} + \frac{C_2}{C_1}$

27. Ans: (d)

Sol: The deviation in the frequency of oscillation of oscillator is due to variation in

(1) Circuit component

(2) Transistor parameters

(3) temperature

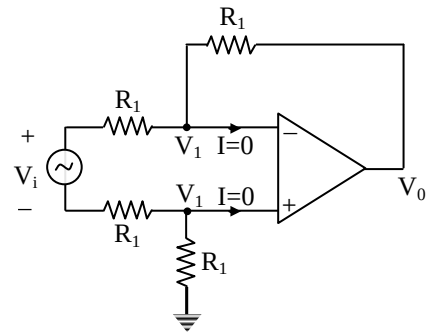
(4) Supply voltage

(5) load

(6) Stray capacitance

28. Ans: (d)

Sol:



Applying KVL at inverting node

$$\frac{V_1 - V_0}{R_1} + \frac{V_1 - V_i - V_1}{2R_1} = 0$$

$$\frac{V_1 - V_0}{R_1} = \frac{V_i}{2R_1}$$

$$V_1 - V_0 = \frac{V_i}{2}$$

Applying KVL at non inverting node

$$\frac{V_1 + V_i - V_1}{2R_1} + \frac{V_1}{R_1} = 0$$

$$\frac{V_i}{2} = -V_1$$

$$\frac{-V_i}{2} - V_0 = \frac{V_i}{2}$$

$$\frac{-V_i}{2} - \frac{V_i}{2} = V_0$$

$$\frac{V_0}{V_i} = -1$$

29. Ans: (a)

Sol: $T = 2RC \ln\left[\frac{1+\beta}{1-\beta}\right]$

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{1}{2} = 0.5$$

$$T = 2 \times 50\ k\ (0.01\ \mu F) \ln\left(\frac{1+0.5}{1-0.5}\right)$$

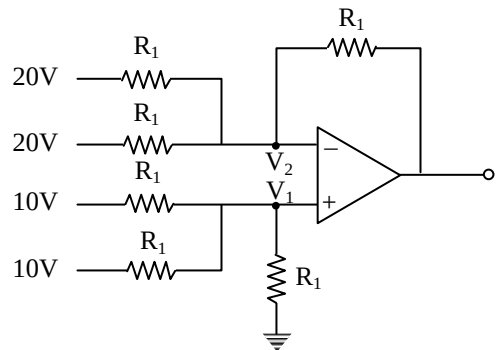
$$= 100k\ (0.01\mu) \ln 3$$

$$= 10^{-3} \ln 3$$

$$f = \frac{1}{T} = \frac{1k}{\ln 3}$$

30. Ans: (d)

Sol:



Applying KVL at non inverting node

$$\frac{V_1 - 10}{R_1} + \frac{V_1 - 10}{R_1} + \frac{V_1}{R_1} = 0$$

$V_1(3) = 20$

$$V_1 = \frac{20}{3}$$

Applying inverting node

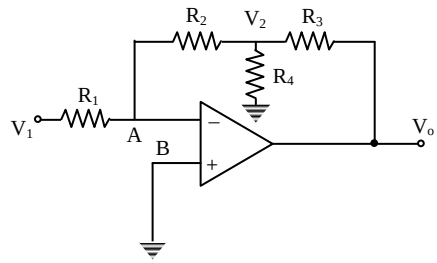
$$\frac{V_1 - 20}{R_1} + \frac{V_1 - 20}{R_1} + \frac{V_1 - V_0}{R_1} = 0$$

$3V_1 - 40 = V_0$

$20 - 40 = -20$

31. Ans: (a)

Sol:



$$V_A = V_B = 0$$

$$\frac{0 - V_1}{R_1} + \frac{0 - V_2}{R_2} = 0 \quad \text{.....} (1)$$

$$\frac{V_2 - 0}{R_2} + \frac{V_2 - V_0}{R_3} + \frac{V_2 - 0}{R_4} = 0 \quad \text{.....} (2)$$

$$V_1 R_2 = -V_2 R_1 \quad \text{.....} (3)$$

$$V_2[R_3 R_4 + R_2 R_4 + R_2 R_3] = V_0 R_2 R_4$$

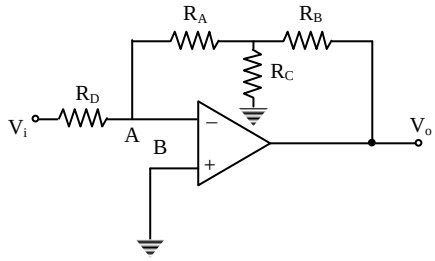
$$V_0 = V_2\left(\frac{R_3}{R_2} + 1 + \frac{R_3}{R_4}\right) \quad \text{.....} (4)$$

$$V_2 = -V_1 . \frac{R_2}{R_1} \text{ sub in } (4)$$

$$V_0 = -\frac{V_1}{R_1}\left(R_2 + R_3 + \frac{R_2 R_3}{R_4}\right)$$

$$= \frac{-\left(R_2 + R_3 + \frac{R_2 R_3}{R_4}\right)}{R_1}$$

SHORT CUT



$$\text{Gain} = \frac{-\left(R_A + R_B + \frac{R_A R_B}{R_C}\right)}{R_D}$$

32. Ans: (a)

Sol: 1. Input resistance is infinity

2. Output resistance is zero

3. Input offset current is zero

4. Band width of the amplifier is infinite

5. CMRR should be infinite.

33. Ans: (b)

Sol: It acts as Miller circuit

Input capacitance $C_{in} = C(1 - A)$

Output capacitance $C_o = \frac{C(A-1)}{A}$

34. Ans: (b)

Sol: $S.R = 2\pi f_{max} V_{0max}$

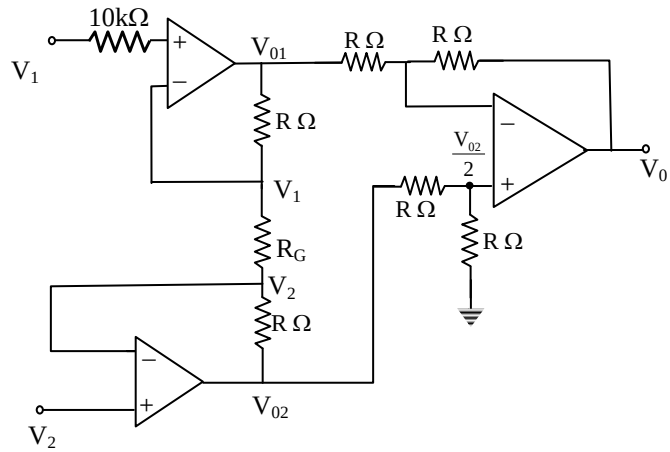
$$= \frac{2\pi \times 10^3}{2}.3$$

$$= 3\pi \times 10^3 \, V/\text{sec}$$

$$= 3\pi \times 10^{-3} \, V/\mu\text{sec}$$

35. Ans: (d)

Sol:



$$\frac{V_1 - V_{01}}{R} + \frac{V_1 - V_2}{R_G} = 0 \qquad \ldots\ldots\ldots (1)$$

$$\frac{V_2 - V_{02}}{R} + \frac{V_2 - V_1}{R_G} = 0 \qquad \ldots\ldots\ldots (2)$$

Eq. (1) – Eq. (2)

$V_1 - V_2 - V_{01} + V_{02} + 2V_1 - 2V_2 = 0$

$3V_2 - 3V_1 = V_{02} - V_{01}$

$$V_0 = -V_{01} + \frac{V_{02}}{2}(1+1)$$

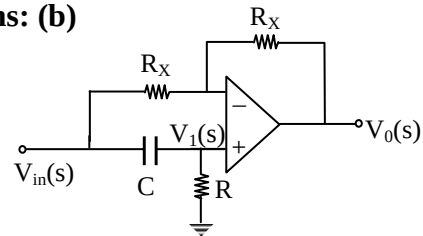
$= V_{02} - V_{01}$

$= 3(V_2 - V_1)$

$= 3(5 - 10) = -15$

36. Ans: (b)

Sol:



$$V_1(s) = V_{in}(s)\frac{R}{R + 1/sc}$$

$$\frac{V_1(s)-V_0(s)}{R_x}+\frac{V_1(s)-V_{in}(s)}{R_x}=0$$

$$2V_1(s)=V_0(s)+V_{in}(s)$$

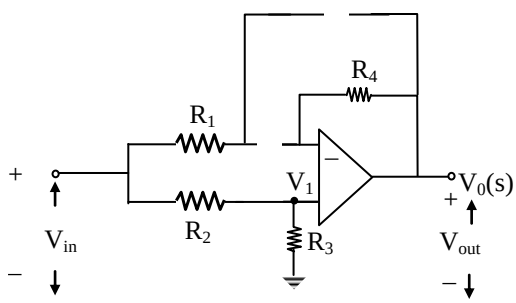
$$V_{in}(s)\frac{2R}{R+\frac{1}{sc}}-V_{in}(s)=V_0(s)$$

$$H(s)=\frac{V_0(s)}{V_{in}(s)}$$

$$=\frac{R-1/sc}{R+\frac{1}{sc}}$$

37. Ans: (c)

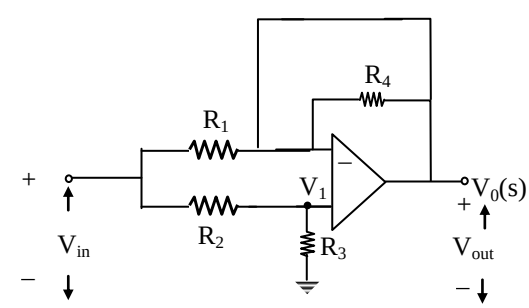
Sol: At f = 0 capacitors will be open circuited.



$$V_1=\frac{R_3}{R_2+R_3}\times V_{in}$$

$$V_0=V_1=\frac{R_3}{R_2+R_3}\times V_{in}$$

At f = ∞ capacitors will be acted like short circuited.



$$V_1=\frac{R_3}{R_2+R_3}\times V_{in}$$

$$V_0=V_1=\frac{R_3}{R_2+R_3}\times V_{in}$$

So the given filter is the band stop filter.

38. Ans: (c)

Sol: Truth table of comparator:

A	B	A = B	A < B	A > B
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

$$X=A\overline{B}=A>B$$

$$Y=\overline{A}B=A<B$$

$$Z=A\odot B=A=B$$

$\therefore$ It is a comparator

39. Ans: (d)

Sol: $f(A,B,C,D)=AB+B\overline{C}+BD$

f(A,B,C,D)

AB \ CD	00	01	11	10
00				
01	1	1	1	
11	1	1	1	1
10				

$\overline{f(A,B,C,D)}$

AB \ CD	00	01	11	10
00	1	1	1	1
01				1
11				
10	1	1	1	1

$\therefore$ Number of minters in $\overline{f(A,B,C,D)}$ is 9.

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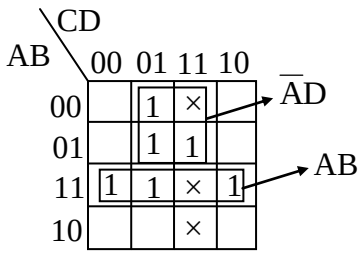
40 Ans: (c)

Sol: f(A,B,C,D) = Σm(1, 5, 7, 12, 13, 14)+d(3, 11, 15)



$f(A,B,C,D) = AB + \overline{A}D$

For the input 0011, f = (0.0)+(1.1) = 1

For the input 1011, f = (1.0)+(0.1) = 0

41. Ans: (c)

Sol: Minimization of Boolean expression is reducing complexity and cost of system. It reduces number of gates required for implementation and also number of inputs (fan-in) of gates.

42. Ans: (d)

Sol: A synchronous counter state changes in one Flipflop delay, if it is changing from one state to another state.The propagation delay is independent of number of bits.

$\therefore$ The maximum time required is 10ns.

43. Ans: (c)

Sol: Synchronous counter will provide clock at a time to all flip flops. Hence it provides least delay.

44. Ans: (a)

Sol: It is mod 12 counter .

After 300 clock cycles

300% 12 = 0

So the state after 300 clock cycles is initial state only.

So $Q_3\ Q_2\ Q_1\ Q_0$ state after 300 clock cycles is 0000.

45. Ans: (b)

Sol: It is a ring counter . So $D_3=Q_0$, $D_2 = Q_3$, $D_1 = Q_2$, $D_0= Q_1$

Q_3	Q_2	Q_1	Q_0
1	0	1	0
0	1	0	1
1	0	1	0

The modulus of counter is '2'

46. Ans: (d)

Sol: $Z = \overline{C}\,\overline{D}\,\overline{A}\,\overline{B} + \overline{C}D(\overline{A}B + A\overline{B}) + CDAB$

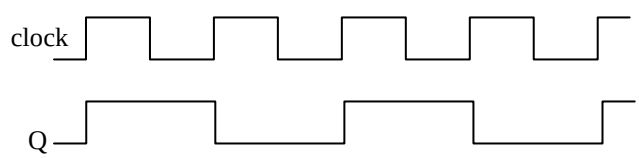
$= \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}D + AB\overline{C}D + ABCD$

$= \sum m(0,5,13,15)$

47. Ans: (c)

Sol: The circuit is SR flip flop with $S = \overline{Q}$ and R = Q.

So the output Q is complementing at every clock cycle



$T_Q = 2T$

$$f_Q = \frac{1}{2T} = \frac{f}{2}$$

$$= \frac{1GHz}{2} = 0.5GHz$$

48. Ans: (c)

Sol: Resolution = $\frac{100-0}{2^6-1} = \frac{100}{63}$ rpm

The number of steps required for 50 speed is

$$= \frac{50}{100/63} \approx 32_{10}$$

$= 100000_2$

49. Ans: (b)

Sol: A dual slope ADC integrates an unknown input voltage (V_{in}) for a fixed amount of time (T_{int}), then de-integrates ($T_{De\text{-}int}$) using a known reference voltage (V_{REF}) for a variable amount of time.

T_{INT} is fixed

$$T_{DE\text{-}int} \propto \frac{V_{IN}}{V_{REF}}$$

Any error introduced by a component value during the integrate cycle will be cancelled out during the de-integrate phase.

$\therefore$ De-integration time period is variable and depends on number of pulses counted during 1st integration.

50. Ans: (B)

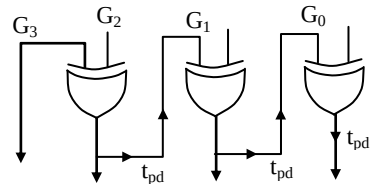
Sol: Resolution = 0.01% = $\frac{0.01}{100}$

$$= \frac{1}{10,000} = \frac{1}{2^n}$$

Minimum number of bits = 14

51. Ans: (b)

Sol: Gray to Binary circuit



$t_{tot} = (N-1)\, t_{pd}$

$= 3\, t_{pd}$

$= 3 \times 2$ nsec

$= 6$nsec

52. Ans: (a)

Sol: MVI B, 00H; [B] = 00H

MVI C, 00H; [C] = 00H

LOOP: DCR C ; [C] = FFH

JNZ LOOP ; Z-flag = 1 so again loop executes till [C] = 00H, i.e 256 times

DCR B ; [B] = FFH

JNZ LOOP ; zero flag = 1 so again loop executes

For [B] = FFH $\rightarrow$ 256 times

For [B] = FEH $\rightarrow$ 256 times

For [B] = FDH → 256 times

⋮

For [B] = 00H → 256 times

∴ Loop executes for 256 × 256 times

53. Ans: (b)

Sol: XRA A ; [A] = 00H, CY = 0

ACI 05H ; [A] = [A] + CY + 05H
= 05H = 00000101

RLC ; [A] = 00001010 = 0AH, CY = 0

MOV B, A ; [B] = 0AH

RLC ; [A] = 00010100, CY = 0

RLC ; [A] = 00101000, CY = 0

ADD B ; [A] ← [A] + [B]

0 0 1 0 1 0 0 0

0 0 0 0 1 0 1 0

+

0 0 1 1 0 0 1 0 = 32H

MOV C, A ; [C] = 32H

54. Ans: (b)

Sol: The time delay for JNZ is 10T if it satisfies the condition otherwise it is 7T.

LOOP executes till the content of C register becomes 0, i.e., for 5 times.

For the first four times JNZ condition will not satisfies, so this instruction will take 10T states.

But during 5th time, JNZ satisfies, which takes 7T states.

Delay = $T_O + T_L - 3T$

= 14T + (5×26T) –3T = 141 T

55. Ans: (c)

Sol: 1. READY is active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

2. ALE is high only during T1. when ALE goes low, the address is saved and AD7-AD0 lines can be used for their purpose as the bi-directional data lines.

∴ Statements (1) and (2) are false.

56. Ans: (c)

Sol: DSBSC Signal

$S(t) = m(t).\cos\omega_c t$

if m(t) signal cross zero i.e m(t) voltage changes from +ve to –ve

for m(t) > 0

assume $S(t) = k\cos\omega_c t$ (here k is positive)

for m(t) < 0

$S(t) = -k\cos\omega_c t$

$= k\cos(\omega_c t + \pi)$

$(\because \cos(\pi+\theta) = -\cos\theta)$

Therefore the modulated wave undergoes phases reversal (π-radians) whenever m(t) (modulating signal) crosses zero.

57. Ans: (b)

Sol: TRAP is represented as RST 4.5

$\therefore$ Vector location = 4.5×8 = 36 D

In Hexadecimal, 36 D = 24 H

58. Ans (b)

Sol: Accumulator = 11010100 (-43_{10})

RLC ---- 10101001 cy = 1

RRC ---- 11010100 cy = 1

RAL----- 10101001(-86_{10}) cy = 1

59. Ans: (b)

Sol: Hardware interrupts in decreasing order of priority:

TRAP

RST 7.5

RST 6.5

RST 5.5

INTR

60. Ans: (d)

Sol: HL register is primary data pointer register used to hold address of a memory location in data RAM.

61. Ans: (b)

Sol: For Compare instruction execution, 8085's ALU performs subtraction operation but result is not saved into accumulator.

$\therefore$ Accumulator is unaltered.

62. Ans: (b)

Sol: The DSB-SC signal is multiplied with carrier of phase angle θ.

$\Rightarrow$ **[**$m(t)\cos\omega_c t]\cos(\omega_c t+\theta)$

$$=\frac{m(t)}{2}[\cos(2\omega_c t+\theta)+\cos\theta]$$

The output of the coherent detector is

$$\frac{m(t)}{2}\cos\theta$$

When $\theta = 60^0$, then output is $\frac{m(t)}{4}$

63. Ans: (c)

Sol: $\beta_f = \frac{\Delta f}{f_m}$

Carrier swing $2\Delta f$ = 100 kHz

$\Rightarrow \Delta f$ = 50 kHz

f_m = 8 kHz

$$\beta_f = \frac{50k}{8k} = 6.25$$

64. Ans: (b)

Sol: Too high IF value would result in poor selectivity, which implies poor adjacent channel rejection. Assume that IF instead of standard 455 kHz if a very high value of 2MHz is considered with bandwidth either 10 kHz or less than 10 kHz than we require very sharp cut-off filters which also increases the cost of the receiver.

Design of such filters is very complex.

65. Ans: (a)

Sol: If the input to the quantizer 0^+ the output voltage +5V and if the input is 0^-, the output is –5V. So, the quantization error varies from –5V to +5V.

66. Ans: (b)

Sol: Bandwidth is decreases by 2/3 in VSB, but bandwidth is decreases by 1/2 in SSB. So option 1 is wrong. And in VSB it is a condition that it should avoids phase distortion at low frequencies.

67. Ans: (b)

Sol:

1. Slope overload distortion occurs in DM.
2. Sampling frequency in DM is far greater than sampling frequency in PCM. So DM has larger bandwidth.
3. DM has simple circuitry.
4. DM has poor performance compared to PCM.

68. Ans: (b)

Sol: Carrier Amplitude $A_c = 6$;

Average power:

$$P_{avg} = \frac{A_c^2}{2R};\ R = 1\Omega$$

$$P_{avg} = \frac{A_c^2}{2R} = \frac{6^2}{2} = 18\ W$$

69. Ans: (d)

Sol: DMA is a process where the data is transferred between two peripherals directly without the involvement of the microprocessor.

$\therefore$ Statement (1) is false

70. Ans: (a)

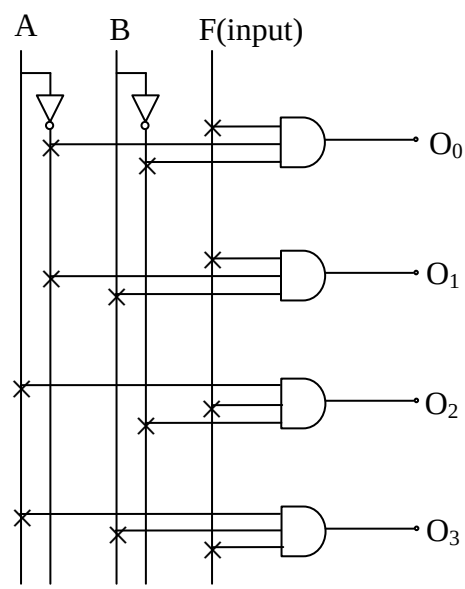
Sol: Power of angle modulated signal depends only on the amplitude of the carrier. So, both statement I, statement II are true and statement II is correct explanation of statement I.

71. Ans: (d)

Sol: Both DSB & SSB have identical noise performance. Statement-I is false and statement-II is correct.

72. Ans: (b)

Sol: Demultiplexer using AND gates



Where A, B are control inputs

O_0, O_1,O_2, O_3 are outputs

A demultiplexer can be used as decoder and demultiplexer can be built by AND gates.

Statement (I) is true. Statement (II) is also true, but not giving correct explanation for I

73. Ans: (b)

Sol: **Statement (I):** At low frequency the gain of R-C coupled amplifier decreases due to the finite impedance of coupling, bypass capacitances.

Statement (II): Parasitic capacitance of active device, winding capacitances effect the gain of the system at high frequency.

74. Ans: (c)

Sol: As the temperature ⇑

1. Depletion layers width ⇓, channel width⇑, Hence current⇑.
2. Carrier mobility ⇓, Resistance of channel ⇑, current ⇓ both 1 & 2 are opposite effects to each other.

75. Ans: (a)

Sol: **Statement (I):** Compared to JET and BJT MOSFET has high input impedance.

Statement (II): Due to SiO_2 layer between gate and channel, it has high input impedance.

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