TEST ID: 101

ACE
Engineering Academy

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ESE- 2019 (Prelims) - Offline Test Series Test-1

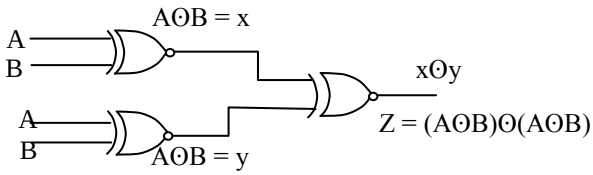
ELECTRONICS & TELECOMMUNICATION ENGINEERING

SUBJECT: ANALOG ELECTRONICS AND DIGITAL ELECTRONICS AND MICRO PROCESSORS

SOLUTIONS

01. Ans: (b)

Sol: The given circuit can be redrawn as below

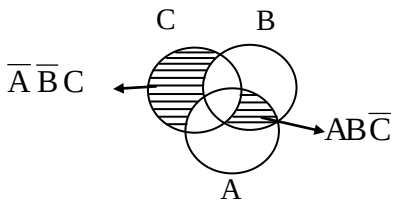


XNOR of equal inputs is '1'

$\Rightarrow Z = 1$

02. Ans: (b)

Sol:



The common area occupied by the given venn diagram is equivalent to its Boolean expression = $\overline{A}\,\overline{B}\,C + AB\overline{C}$

03. Ans: (c)

Sol: Truth table of comparator:

A	B	A = B	A < B	A > B
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

$X = A\overline{B} \Rightarrow A > B$

$Y = \overline{A}B \Rightarrow A < B$

$Z = A \odot B \Rightarrow A = B$

$\therefore$ It is a comparator

04. Ans: (c)

Sol: Minimization of Boolean expression is reducing complexity and cost of system. It reduces number of gates required for implementation and also number of inputs (fan-in) of gates.

05. Ans: (d)

Sol: $f(A, B, C, D) = AB + B\overline{C} + BD$

f(A,B,C,D)

AB \ CD	00	01	11	10
00				
01	1	1	1	
11	1	1	1	1
10				

$\overline{f(A, B, C, D)}$

AB \ CD	00	01	11	10
00	1	1	1	1
01				1
11				
10	1	1	1	1

$\therefore$ number of minters in $\overline{f(A, B, C, D)}$ is 9.

06. Ans: (a)

Sol: The range of decimal integers can be represented using n bits is -2^{n-1} to $+(2^{n-1}-1)$

The range of decimal integers using 9 bits is -2^{9-1} to $(2^{9-1}-1)$ i.e., – 256 to +255.

07. Ans: (a)

Sol: The F's complement of hexadecimal number C091.20F30

$$\text{F's complement} \Rightarrow \begin{array}{rr} & \text{FFFF . FFFFF} \\ (-) & \text{C091 . 20F30} \\ \hline & \text{3F6E . DF0CF} \end{array}$$

08. Ans: (a)

Sol: It is mod 12 counter .
After 300 clock cycles

300% 12 = 0
So, the state after 300 clock cycles is initial state only.
So, $Q_3\ Q_2\ Q_1\ Q_0$ state after 300 clock cycles is 0000.

09. Ans: (d)

Sol: A synchronous counter state changes in one Flipflop delay, if it is changing from one state to another state. The propagation delay is independent of number of bits.
$\therefore$ The maximum time required is 10ns.

10. Ans: (b)

Sol: It is a ring counter . So $D_3=Q_0$, $D_2 = Q_3$, $D_1 = Q_2$, $D_0= Q_1$

Q_3	Q_2	Q_1	Q_0
1	0	1	0
0	1	0	1
1	0	1	0

The modulus of counter is '2'

11. Ans: (c)

Sol: The size of the ROM = $128\times8 = 2^7\times8$
$\Rightarrow$The total number of bits need not to be programmed = $[2^7\times8] - [2^6\times6]$
$= 2^6\,[(2\times8) - 6]$
$= 64\times10$
$= 640$

12. Ans: (d)

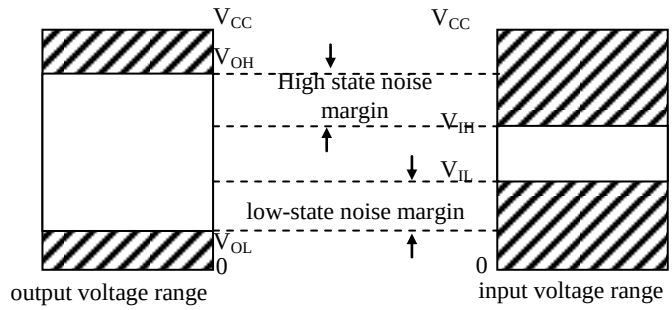
Sol: The capacity of PLA is specified by the number of inputs, number of product terms and number of outputs.

13. Ans: (c)

Sol: MOS logic offers low power consumption. Because of the low voltage requirement, it is highly suitable for battery operated systems.
MOS logic has highest packing density and high fan-out

14. Ans: (b)

Sol:



From the signals for evaluating noise margin shown above,
$V_{OH} > V_{IH}$
$V_{IL} > V_{OL}$
$V_{OH} > V_{OL}$
$V_{IH} > V_{IL}$
$\therefore$ option (b) is incorrect

15. Ans: (c)

Sol: For hard real-time systems, no deadline misses are tolerated. For soft real-time systems, it is acceptable for tasks to miss deadlines occasionally and tasks not finished by their deadlines are still completed, albeit with reduced values. Firm real-time systems also allow occasional deadline misses.

16. Ans: (d)

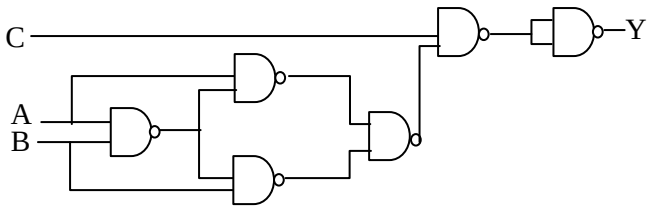
Sol: $Z = \overline{C}\,\overline{D}\,\overline{A}\,\overline{B} + \overline{C}D\left(\overline{A}B + A\overline{B}\right) + CDAB$

$= \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}D + AB\overline{C}D + ABCD$

$= \sum m(0,5,13,15)$

17. Ans: (b)

Sol: (A) $Y = A\overline{B}C + \overline{A}BC = (A \oplus B)C$



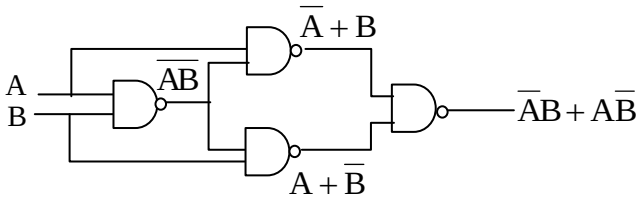
For Y operation 6 NAND gates are required

(B) $Y = \overline{AB} + AB + \overline{C} = 1 + \overline{C} = 1$

No need of NAND gate

(C) $Y = A\overline{B}[1 + C] + \overline{A}B$

$Y = A \oplus B$



4 NAND gates are required.

18. Ans: (a)

Sol: AB + BC + AC is a self dual function

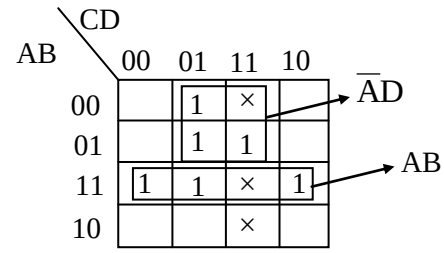
AB + BC + AC is carry output of full adder

AB + BC + AC is resulting output 1 when number of 1's are more

Full subtractor borrow expression is = $\overline{A}B + BC + \overline{A}C$

19. Ans: (c)

Sol: f(A,B,C,D) = Σm(1, 5, 7, 12, 13, 14) + d(3, 11, 15)



$f(A,B,C,D) = AB + \overline{A}D$

For the input 0011, f = (0.0) + (1.1) = 1

For the input 1011, f = (1.0) + (0.1) = 0

20. Ans: (a)

Sol:

2 | 47
2 | 23–1
2 | 11–1
2 | 5 – 1
2 | 2 – 1
1 – 0

+47 = 0 0 1 0 1 1 1 1

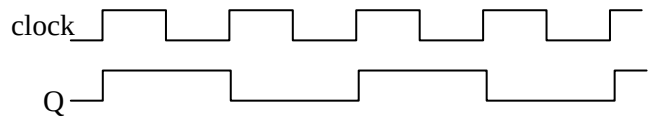
magnitude

sign

21. Ans: (c)

Sol: The circuit is SR flip flop with $S = \overline{Q}$ and R = Q.

So the output Q is complementing at every clock cycle



$T_Q = 2T$

$f_Q = \frac{1}{2T} = \frac{f}{2}$

$= \frac{1GHz}{2} = 0.5GHz$

22. Ans: (c)

Sol: BCD to 7 segment ---combinational circuit

4 to 1 multiplexer ---- combinational circuit

4 bit shift register --- sequential circuit

BCD counter ---- sequential circuit

23. Ans: (c)

Sol: Synchronous counter will provide clock at a time to all flip flops. Hence it provides least delay compared to other counters.

24. Ans: (b)

Sol: (a) Correct statement

R_1 = Resolution of 10 bit digital ramp ADC

$$= \frac{V_{ref}}{2^{10}-1}$$

R_2 = Resolution of 8 bit digital ramp ADC

$$= \frac{V_{ref}}{2^{8}-1}$$

$R_1 < R_2$

R_1 has better resolution than R_2

(b) Conversion time of SAR = nT

That means independent of input voltage, SAR conversion time is always depends on number of bits only

(c) A flash ADC not contains a DAC is also right statement.

(d) VCO is the main component of a voltage to frequency ADC. This also right statement.

25. Ans: (c)

Sol: Resolution = $\frac{100-0}{2^6-1} = \frac{100}{63}$ rpm

The number of steps required for 50 speed is = $\frac{50}{100/63} \approx 32_{10} = 100000_2$

26. Ans: (b)

Sol: Resolution $= 0.01\% = \frac{0.01}{100}$

$$= \frac{1}{10{,}000} = \frac{1}{2^n}$$

Minimum number of bits = 14

27. Ans: (b)

Sol: A dual slope ADC integrates an unknown input voltage (V_{in}) for a fixed amount of time (T_{int}), then de-integrates ($T_{de\text{-}int}$) using a known reference voltage (V_{REF}) for a variable amount of time.

T_{int} is fixed

$$T_{de\text{-}int} \ \alpha \frac{V_{in}}{V_{REF}}$$

Any error introduced by a component value during the integrate cycle will be cancelled out during the de-integrate phase.

$\therefore$ De-integration time period is variable and depends on number of pulses counted during 1st integration.

28. Ans: (a)

Sol:

```
        MVI B,  00H;        [B] = 00H
        MVI C,  00H;        [C] = 00H
LOOP:   DCR C       ;       [C] = FFH
        JNZ LOOP    ; Z-flag = 1 so again loop executes
                      till [C] = 00H, i.e 256 times
        DCR B       ; [B] = FFH
        JNZ LOOP    ; zero flag = 1 so again loop executes
```

For [B] = FFH → 256 times
For [B] = FEH → 256 times
For [B] = FDH → 256 times
⋮
For [B] = 00H → 256 times
∴ loop executes for 256 × 256 times

29. Ans: (b)

Sol:
```
XRA A      ; [A] = 00H, CY = 0
ACI 05H    ; [A] = [A] + CY + 05H
             = 05H = 00000101
RLC        ; [A] = 00001010 = 0AH, CY = 0
MOV B, A   ; [B] = 0AH
RLC        ; [A] = 00010100, CY = 0
RLC        ; [A] = 00101000, CY = 0
ADD B      ; [A] ← [A] + [B]
             0 0 1 0    1 0 0 0
             0 0 0 0    1 0 1 0
             +
             0 0 1 1    0 0 1 0 = 32H
MOV C, A   ; [C] = 32H
```

30. Ans: (c)

Sol: The interrupt vector table consists of 256 number of 4-byte pointers, and resides in the first 1kB of addressable memory. Each interrupt number is reserved for a specific purpose.

31. Ans: (a)

Sol: There are total 9 flags in 8086
(a) conditional or status flags : 6 flags
1. Sign flag (S)
2. Zero flag (Z)
3. Auxiliary carry flag (AC)
4. Parity flag (P)
5. Carry flag (CY)
6 Over flow flag (O)

(b) Control flags : 3 flags
1. Directional flag (D)
2. Interrupt flag (I)
3. Trap flag (T)

32. Ans: (a)

Sol: The flag register (program status word) of 8051 microcontroller is:

CY	AC	F0	RS1	RS0	OV	–	P

Carry flag (CY), auxiliary carry (AC), parity (P) and overflow (OV) are conditional flags.
∴ There is no zero flag in 8051.

33. Ans: (c)

Sol: XRL operand 1, operand2: a bitwise "EXCLUSIVE OR" operation between operand1 and operand 2, leaving the resulting value in operand 1.
Here, operand 1 is [A] = FFH
[A] ← FF ⊕ R6
So, it finds the 1's complement of R6 register.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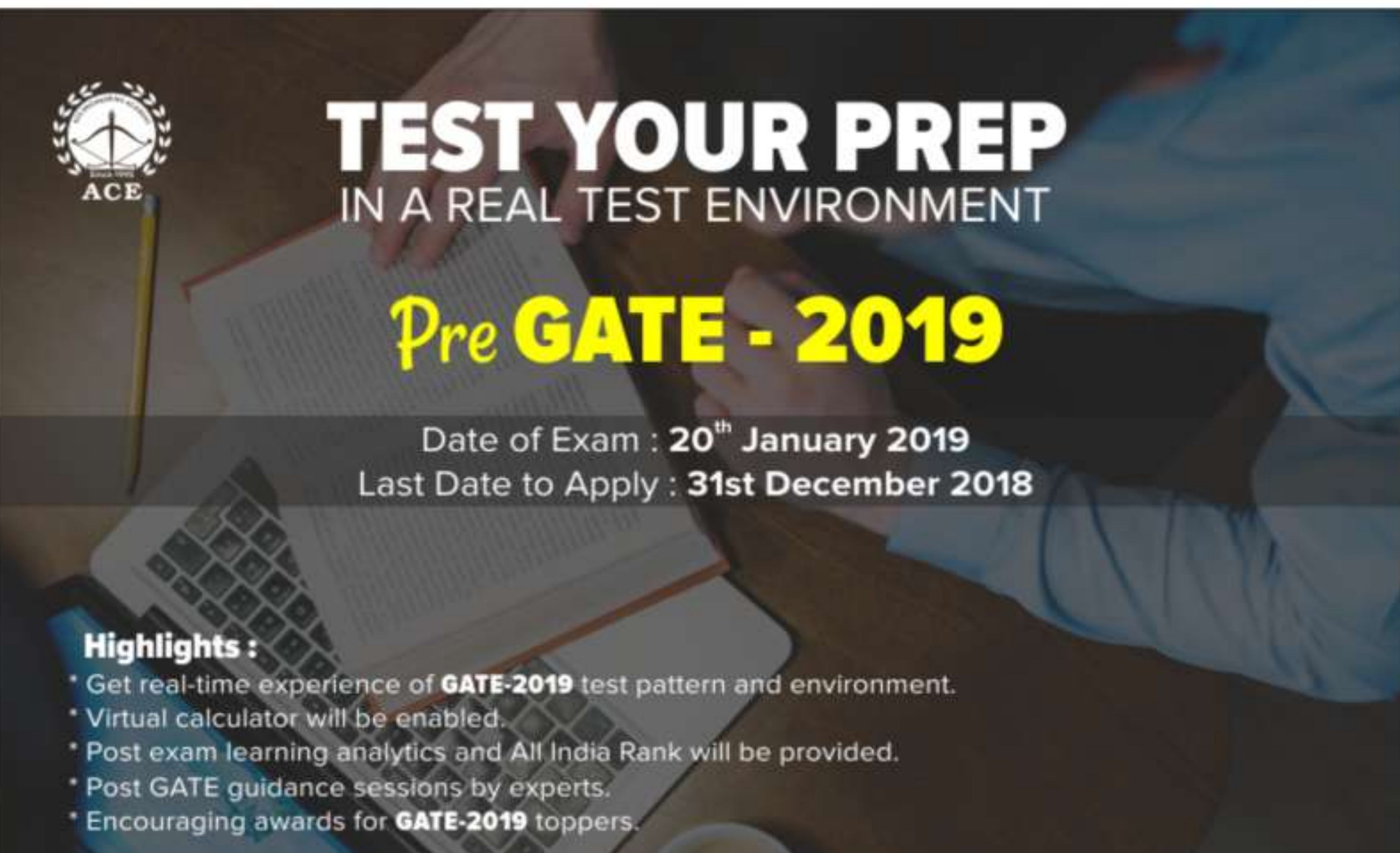
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34. Ans: (b)

Sol: The time delay for JNZ is 10T if it satisfies the condition otherwise it is 7T.

LOOP executes till the content of C register becomes 0, i.e., for 5 times.

For the first four times JNZ condition will not satisfies, so this instruction will take 10T states.

But during 5th time, JNZ satisfies, which takes 7T states.

Delay = $T_O + T_L - 3T$

$= 14T + (5\times 26T) - 3T = 141\ T$

35. Ans: (c)

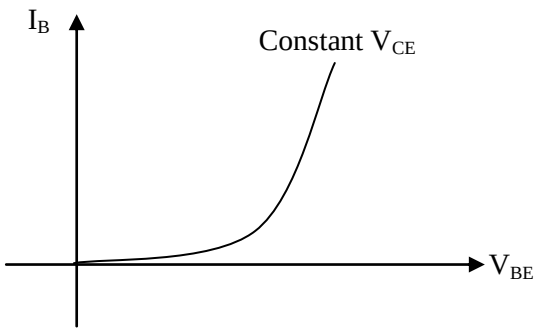
Sol: 1. READY is active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state.

2. ALE is high only during T1. when ALE goes low, the address is saved and AD7 - AD0 lines can be used for their purpose as the bi-directional data lines.

$\therefore$ Statements (1) & (2) are false

36. Ans: (d)

Sol: 1) In Common emitter configuration the input characteristics are plotted between V_{BE} and I_B at constant V_{CE}.



2) Common base configuration is acts as a current buffer whose input resistance is very low(zero ideally). So CB configuration has lower resistance compared to CE.

3) CB configuration has high voltage gain and its current gain is approximately 1.

$\therefore$ Given three statements are incorrect.

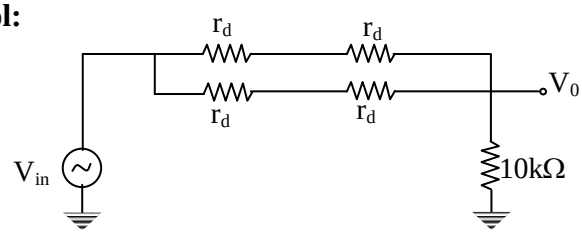
37. Ans: (c)

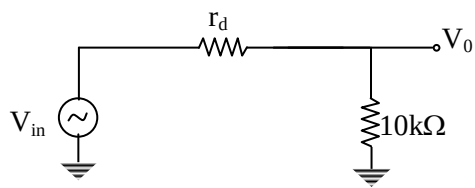
Sol:

Type of power amplifier	Conduction angle
Class-A	360^o
Class-B	180^o
Class-AB	$> 180^o$
Class-C	< 180

38. Ans: (a)

Sol:





$$\frac{V_0}{V_{in}} = \frac{10k}{r_d + 10k}$$

$$r_d = \frac{V_T}{I/2} = \frac{2V_T}{I}$$

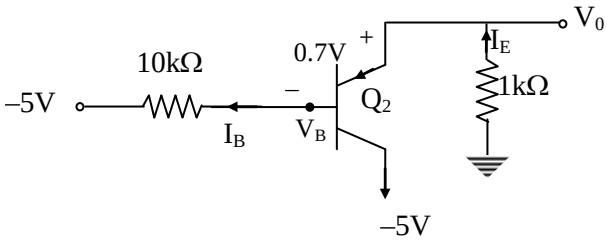
$$I = 5\ \mu A \Rightarrow r_d = \frac{2\times 25mV}{5\mu A} = 10k\Omega$$

$$\frac{V_0}{V_{in}} = \frac{10k}{10k + 10k} = \frac{10}{20} = 0.5\,V/V$$

39. Ans: (b)

Sol: For $V_i = -5V$

(Q_2) gets ON, (Q_1) gets OFF



Q_2 is in active region

$V_B = V_0 - 0.7$

Apply KVL

$I_E + 0.7 + 10I_B - 5 = 0$

$$I_E + 10\left(\frac{I_E}{100}\right) = 5 - 0.7$$

$$I_E = \frac{4.3}{1.1} = 3.9\text{mA}$$

$V_0 = -I_E(1k) = -3.9$ V

40. Ans: (b)

Sol: $$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1\text{mA}}{25\text{mV}} = 0.04\,\text{A/V}$$

$$f_T = \frac{0.04}{2\pi\left(\frac{10\mu + 5\mu}{\pi}\right)} = \frac{4}{100 \times 2 \times 15\mu}$$

$$= \frac{4}{3 \times 10^{-3}} = 1.33\text{kHz}$$

41. Ans: (c)

Sol: Maximum voltage on secondary side

$$V_m = 500\pi\sqrt{2} \times \frac{1}{2} = 250\pi\sqrt{2} \text{ Volts}$$

$$(V_{dC})_{\text{no load}} = \frac{2V_m}{\pi} = \frac{2 \times 250\pi\sqrt{2}}{\pi}$$

$$= 500\sqrt{2} \text{ Volts}$$

42. Ans: (c)

Sol: Negative feedback in OP-amp reduces the voltage gain and makes the linear operations possible.

Oscillations possible with positive feedback.

43. Ans: (d)

Sol: (A) Hartley oscillator : Inductive feedback is used

(B) RC phase shift oscillator : Pure sine wave output is possible

(C) Wein bridge oscillator : Both positive and negative feedback

(D) Colpitt's oscillator : Capacitive feedback is used

44. Ans: (a)

Sol: Given that, $\frac{dA}{A} = \frac{10}{100} = 0.1$

Variation in closed loop gain $\frac{dA_f}{A_f} = \frac{0.1}{100} = 0.001$

Sensitivity factor = $\frac{1}{1 + A\beta}$

Desensitivity factor = $\frac{1}{\text{Sensitivity}} = 1 + A\beta$

$$\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\frac{dA}{A}$$

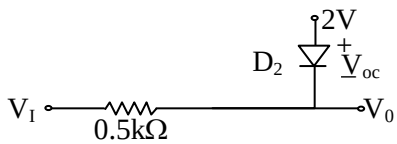
$$0.001 = \frac{1}{1+A\beta}(0.1)$$

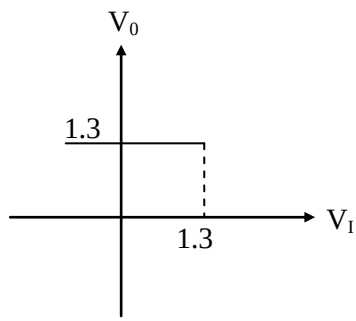
$$1+A\beta = \frac{0.1}{0.001} = 100$$

45. Ans: (b)

Sol: Case: I

Consider D_1 - OFF, D_2 - ON





By KVL

$2 - V_{oc} - V_I = 0 \Rightarrow V_{oc} = 2 - V_I$

For D_2 ON $\Rightarrow V_{oc} > 0.7$

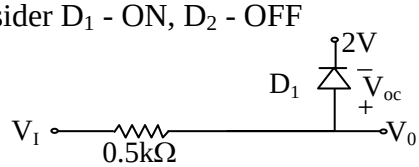
$\Rightarrow 2 - V_I > 0.7$

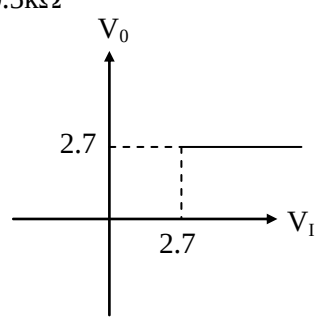
$\Rightarrow V_I < 1.3$

$V_0 = 1.3$ Volts

Case: II

Consider D_1 - ON, D_2 - OFF





By KVL

$2 + V_{oc} - V_I = 0 \Rightarrow V_{oc} = V_I - 2$

For D_1 ON $\Rightarrow V_{oc} > 0.7$

$\Rightarrow V_I - 2 > 0.7$

$\Rightarrow V_I > 2.7$

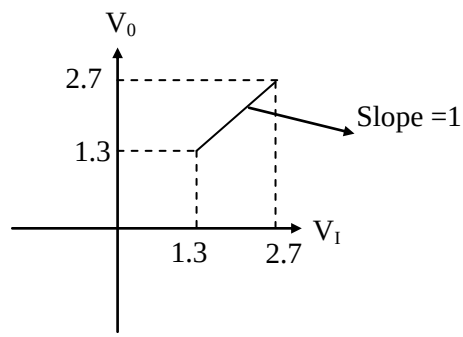
$V_0 = 2.7$ Volts

Case: III

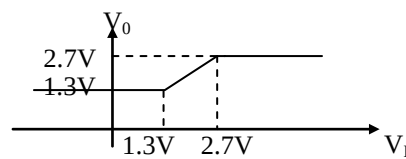
Consider D_1 - OFF & D_2 – OFF

Both diodes are OFF if $1.3 < V_I < 2.7$

Here, $V_I = V_0$



Hence by combining above three cases, the input-output characteristics is



46. Ans: (c)

Sol: $I_{01} = I_{03} = I_{ref}$

$I_{04} = 3I_{ref}$

$I_{02} = 2I_{ref}$

Given that $I_{02} = 200\ \mu A$

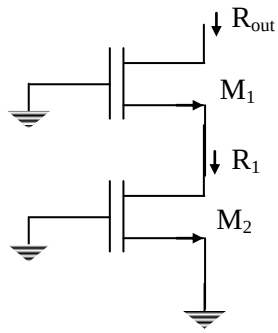
$\Rightarrow I_{ref} = \frac{I_{02}}{2} = 100\ \mu A$

$I_{04} = 3I_{ref} = 300\ \mu A$

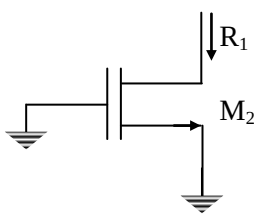
47. Ans: (d)

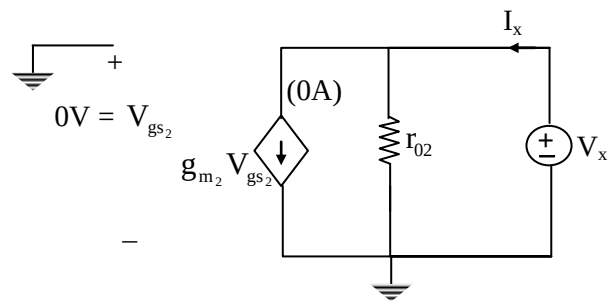
Sol:

Method-1



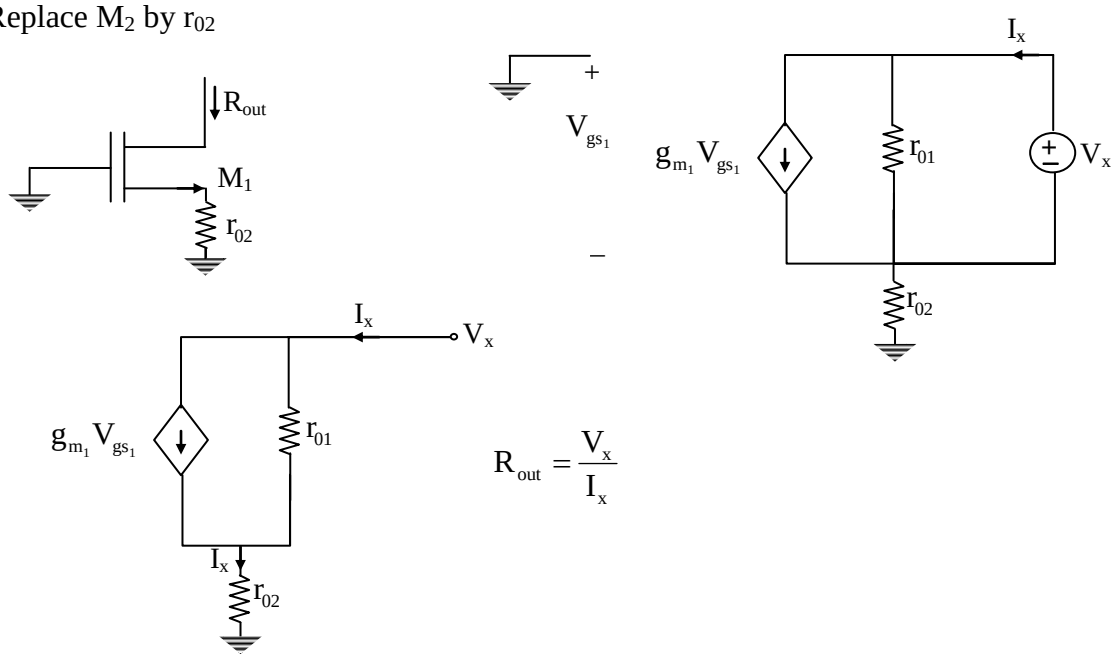
Finding R_1:





$$\frac{V_x}{I_x} = R_1 = r_{02}$$

Replace M_2 by r_{02}



$$R_{out} = \frac{V_x}{I_x}$$

KCL at output node:

$$-I_x + g_{m1}V_{gs1} + \frac{V_x - I_x r_{02}}{r_{01}} = 0$$

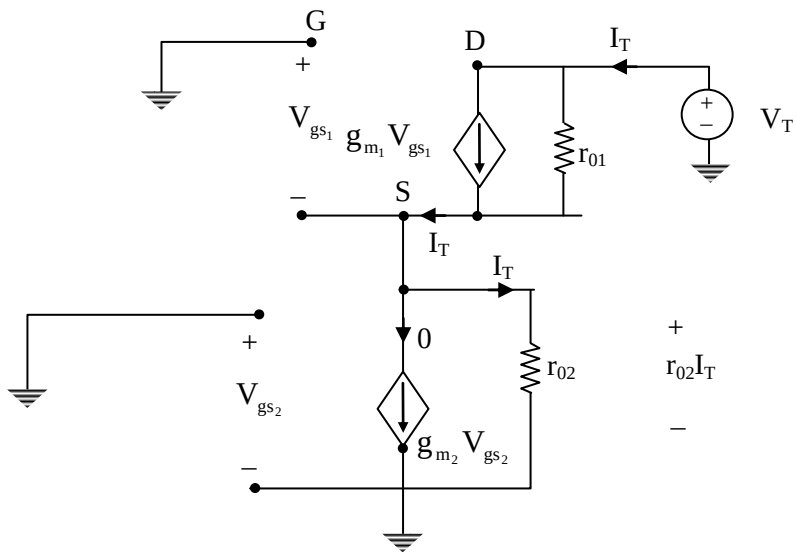
$$-I_x + g_{m1}(0 - I_x r_{02}) + \frac{V_x}{r_{01}} - I_x \frac{r_{02}}{r_{01}} = 0$$

$$\frac{V_x}{r_{01}} = I_x\left[1 + g_{m1}r_{02} + \frac{r_{02}}{r_{01}}\right]$$

$$\frac{V_x}{I_x} = r_{01} + g_{m1}r_{01}r_{02} + r_{02} = R_{out}$$

Method-2

Calculation of output Resistance (R_{out}) ; ($V_{in} = 0$)



Here, $V_{gs_2} = 0 \Rightarrow g_{m_2}V_{gs_2} = 0$

$\Rightarrow -V_{gs_1} - r_{02}I_T = 0 \Rightarrow V_{gs_1} = -r_{02}I_T$

By KVL

$$V_T - r_{01}\left(I_T - g_{m_1}V_{gs_1}\right) - r_{02}I_T = 0$$

$$\Rightarrow V_T = r_{01}I_T + g_{m_1}V_{gs_1}r_{01} + r_{02}I_T$$

$$\Rightarrow V_T = r_{01}I_T + g_{m_1}r_{01}r_{02}I_T + r_{02}I_T$$

$$\Rightarrow \frac{V_T}{I_T} = r_{01} + r_{02} + g_m r_{01}r_{02}$$

$$\Rightarrow R_{out} = \frac{V_T}{I_T} = r_{01} + r_{02} + g_{m_1}r_{01}r_{02}$$

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48. Ans: (a)

Sol: $A_f(0) = \dfrac{A_V}{1+\beta A_V}$

$$100 = \frac{10^4}{1+\beta A_V}$$

$$1+\beta A_V = \frac{10^4}{100} = 100$$

$\omega_{Hf} = \omega_H (1+\beta A_V) = 50 \times 100$

$= 5000$ rad/sec

49. Ans: (c)

Sol: V_{BCO} : Voltage across Base-collector junction when emitter open

$V_{BCO} = 70$ V

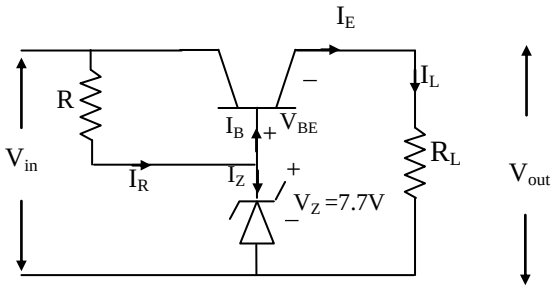
$V_B - V_C\big|_{V_E=\text{open}} = 70V$

$10 - V_0 = 70$

$V_0 = -60$ V

50. Ans: (d)

Sol:



$V_{out} = V_Z - V_{BE} = 7.7 - 0.7 = 7V$

$V_{CE} = V_{in} - V_{out} = 15 - 7 = 8V$

$$I_R = \frac{V_{in} - V_Z}{R}$$

$$= \frac{15-7.7}{7.3k} = 1mA = 1000\mu A$$

$$I_L = \frac{V_{out}}{R_L} = \frac{7}{3.5k} = 2mA$$

$$I_B = \frac{I_E}{1+\beta} = \frac{2m}{100} = 20\mu A \qquad [\because I_E = I_L]$$

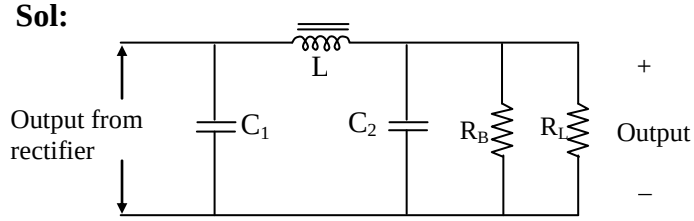
$I_Z = I_R - I_B = 1000\mu - 20\mu = 980\ \mu A$

51. Ans: (d)

Sol: Ripple factor of power supply is a measure of purity of power output.

52. Ans: (d)

Sol:



(i) When actual load is connected, there is a small additional voltage drop. Thus the difference between no load and full load voltage is reduced. Thus, voltage regulation is improved.

(ii) Bleeder resistor improves the filtering action by maintaining a minimum current through the choke

(iii) When a bleeder is not used and power supply is switched off, the capacitor retains its charge for some time which is dangerous for people working with equipment. This high voltage discharges through bleeder.

53. Ans: (b)

Sol: In class B

$\rightarrow$ For low signal voltage, Ic = 0

$\rightarrow$ Cross- over distortion problem is there

In class AB

$\rightarrow$ Even for no signal, small current flows

Hence power drawn is not zero

54. Ans: (b)

Sol: Monolithic ICs offer low power rating. So, statement(iii) is wrong statement.

55. Ans: (a)

Sol: (A) Thin and thick layer IC s are also known as printed film circuits because in their manufacturing silk-screen printing techniques are used.

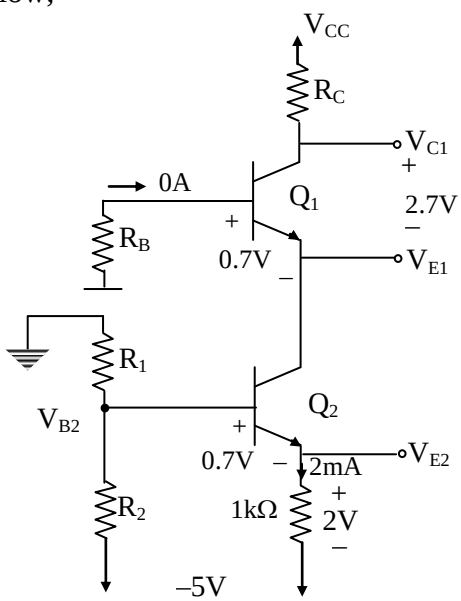
(B) Hybrid IC is combination of number of monolithic IC's. These are widely used for high power audio amplifier applications.

(C) Linear IC's input and output relationship is linear. So used in amplifiers, oscillators etc

(D) Digital IC's find wide applications in computers and logic circuits.

56. Ans: (a)

Sol: $\beta = \infty$, i.e. base currents are zero for both Q_1 & Q_2. So, the circuit can be redrawn as below,



$V_{E2} = -5 + (2m \times 1k) = -3V$

$V_{BE2} = 0.7V$

$V_{B2} - V_{E2} = 0.7$

$\Rightarrow V_{B2} = 0.7 + V_{E2} = 0.7 - 3$

$V_{B2} = -2.3V$

$V_{BE1} = 0.7\ V$

$V_{B1} - V_{E1} = 0.7$

$0 - V_{E1} = 0.7$

$V_{E1} = -0.7\ V$

Given that $V_{CE1} = 2.7\ V$

$V_{C1} - V_{E1} = 2.7\ V$

$V_{C1} = 2.7 + V_{E1}$

$= 2.7 - 0.7$

$= 2\ V$

$$\frac{V_{E2}}{V_{C1}} = \frac{-3}{2} = -1.5$$

57. Ans: (b)

Sol: $-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E}$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{1+\beta}{1-\beta\dfrac{dI_B}{dI_C}}$$

$$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_E + R_B}}$$

$$= \frac{1+99}{1+99\left(\dfrac{1}{10}\right)}$$

$$= \frac{100}{10.9}$$

$$= 9.17$$

58. Ans: (d)

Sol: The node at which input is given is same as the feedback taken node. So shunt at input. If the feedback node is at one node and output taken from another node, then it is said to be Series at output.

59. Ans: (c)

Sol: $i_D = \frac{1}{2}K'_n \frac{W}{L}(V_{GS} - V_T)^2$

At $i_D = 1mA$

$\Rightarrow 1m = \frac{1}{2}K'_n \frac{W}{L}(-1 - V_T)^2$ ……..(1)

At $i_D = 9mA$

$\Rightarrow 9m = \frac{1}{2}K'_n \frac{W}{L}(1 - V_T)^2$ ……..(2)

$\frac{(2)}{(1)} \Rightarrow \frac{9}{1} = \frac{(1-V_T)^2}{(1+V_T)^2}$

$\frac{1-V_T}{1+V_T} = \pm 3$

$\frac{1-V_T}{1+V_T} = 3$ $\qquad$ $\frac{1-V_T}{1+V_T} = -3$

$1-V_T = 3+3V_T$ $\qquad$ $1-V_T = -3-3V_T$

$4V_T = -2$ $\qquad$ $-2V_T = 4$

$V_T = -0.5V$ $\qquad$ $V_T = -2V$

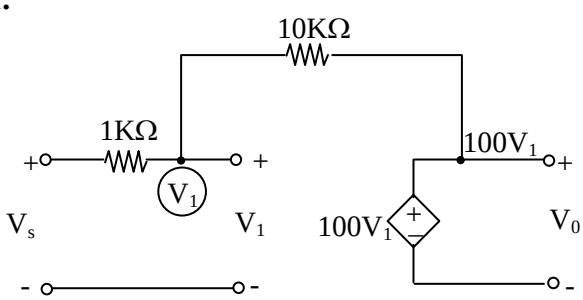
$V_{GS} = -1V < V_T$

So $V_T = -0.5$ not possible

$\therefore V_T = -2V$

60. Ans: (d)

Sol:



KCL

$\frac{V_S - V_1}{1K} = \frac{V_1 - 100V_1}{10K}$

$10V_S - 10V_1 = -99V_1$

$10V_S = -89V_1$

$\rightarrow V_1 = \frac{-10}{89}V_S$

$V_0 = 100V_1 = 100\left[\frac{-10}{89}\right]V_S$

$\frac{V_0}{V_S} = \frac{-1000}{89}$

61. Ans: (d)

Sol: $\beta = \frac{SL_1}{SL_2} = \frac{L_1}{L_2}$

$A = \frac{-R_F}{R_1}$; $A = \frac{1}{\beta}$ for sustained oscillations)

$\left|\frac{-R_F}{R_1}\right| = \frac{L_2}{L_1}$

$\frac{R_F}{2k} = \frac{5mH}{2mH}$

$R_F = 5k\Omega$

62. Ans: (b)

Sol: 1. In 555 timers, threshold level is $\frac{2}{3}V_{CC}$

2. –ve trigger pulse is required to change the output state in monostable multivibrator
3. One of the application of 555 in Astable modes FSK generation
4. In Schmitt trigger using 555 timer, $V_{UTP} = \frac{V_{CC}}{6}$ and $V_{LTP} = -\frac{V_{CC}}{6}$

63. Ans: (b)

Sol: Step (1):

Effective voltage applied at the inverting input terminal of op-amp

$= \frac{10k \times 12V}{10k + 10k} = 6V$ ---- (1)

Step (2):

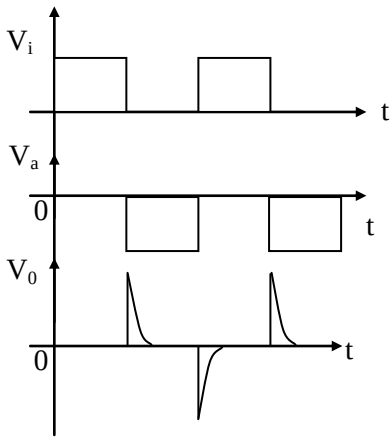
For the output of op-amp to be positive, the input at non-inverting terminal of op-amp should of more than 6 V, i.e $V_i > 6$ V---- (2)

Step (3):

In the op-amp circuit shown, for the LED to turn ON, the output of op-amp should be positive. To get this +ve output, $V_i > 6$ V

64. Ans: (c)

Sol: In the circuit a half wave rectifier and a differentiator is cascaded when we give a square-wave input to the half-wave rectifier, the output voltage V_0 is shown below.



The differentiator, the voltage V_a is to be differentiate and results a output voltage, V_0 which is impulse (spikes) wave as shown above.

65. Ans: (c)

Sol: Voltage at non-inverting terminal

$$V_p = \frac{V_1 + V_2 + V_3 + V_4}{4}$$

$$V_P\left[\frac{1}{R} + \frac{1}{R_f}\right] = \frac{V_0}{R_f}$$

$$\frac{1}{4}\left[\frac{1}{R} + \frac{1}{R_f}\right] = \frac{1}{R_f}$$

$$\Rightarrow \frac{1}{R} + \frac{1}{R_f} = \frac{4}{R_f}$$

$$\Rightarrow R = \frac{R_f}{3}$$

66. Ans: (b)

Sol: $\rightarrow$ JFET has low resistance (R_{GS}) compared to MOSFET.

So, the statement (a) is wrong.

$\rightarrow$ g_m of JFET is maximum when $V_{GS}= 0$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

The above g_m is maximum when $V_{GS} = 0$

$\rightarrow$ Elbers-Moll model can be used for both npn and pnp transistors

$\rightarrow$ Usually FET has infinite resistance between gate and source

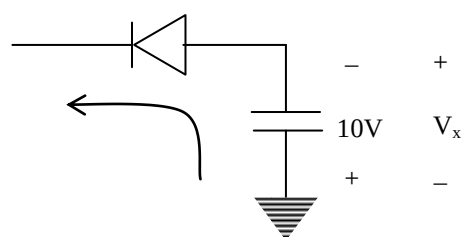
67. Ans: (b)

Sol: The Gate can be self aligned to source and drain in a MOSFET with polysilicon gate.

So it is preferred than a MOSFET with Aluminium gate. Overload and peak current handling capability is high

68. Ans: (d)

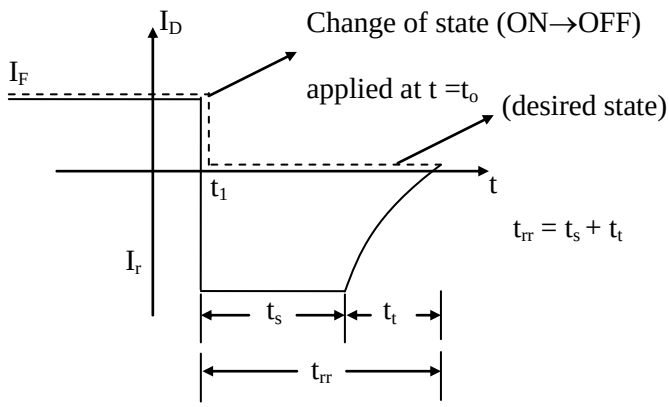
Sol: Positive cycle the first capacitor charges to peak of 5v, During negative cycle D_1 is RB, D_2 is FB capacitor charges to 10V in the polarity shown



Therefore $V_x = -10V$

69. Ans: (c)

Sol: Reverse recovery time (t_{rr}):



Where t_{rr}: reverse recovery time

t_s: Storage time

t_t: transition time

Diffusion capacitance exist in forward bias-region and transition capacitance exist in reverse-bias region.

70. Ans: (c)

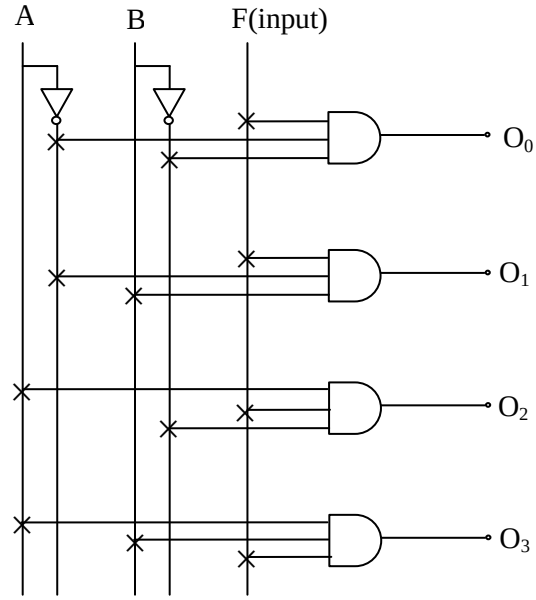
Sol: (1) The cross over distortion is eliminated in a push-pull amplifier by providing a small forward bias to the transistor.

(2) The harmonic distortion refers to the non-sinusoidal nature of a periodic wave form and it defined at periodic frequency and multiple of that frequency.

∴The statement(1) and (2) are correct statements.

71. Ans: (b)

Sol: Demultiplexer using AND gates



Where A, B are control inputs

O_0, O_1,O_2, O_3 are outputs

A demultiplexer can be used as decoder and demultiplexer can be built by AND gates.
Statement (I) is true. Statement (II) is also true, but not giving correct explanation for I

72. Ans: (b)

Sol: In I^2L logic all individual transistors of RTL are replaced by multi collector transistors.

∴ Both statements are true but statement(II) is not giving correct explanation for statement(I) .

73. Ans: (d)

Sol: DMA is a process where the data is transferred between two peripherals directly without the involvement of the microprocessor.

∴ statement (I) is false & statement (II) is true

74. Ans: (d)

Sol: Blocking oscillator is a relaxation oscillator which generates short time duration pulse using a transistor as an active device.

$\therefore$ Statement (I) is false.

Blocking oscillators are used to generate pulses of large peak power.

$\therefore$ Statement (II) is true.

75. Ans: (d)

Sol: Zener regulator has low efficiency for heavy load currents as there is a considerable power loss in R.

$$V_{out} = V_Z + I_Z Z_I$$

The regulator is used only when there are small variations in load current and input voltage.

$\therefore$ Statement (I) is wrong and statement (II) is true.

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