

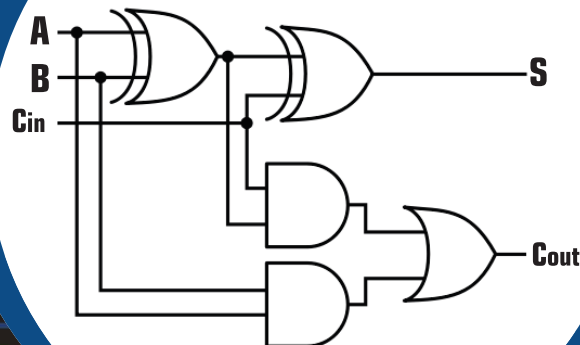


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ELECTRONICS & TELECOMMUNICATION ENGINEERING

DIGITAL CIRCUITS & MICROPROCESSORS

Volume - 1 : Study Material with Classroom Practice Questions



01. Ans: (d)

Sol: $135_x + 144_x = 323_x$

$$(1 \times x^2 + 3 \times x^1 + 5 \times x^0) + (1 \times x^2 + 4 \times x^1 + 4 \times x^0) = 3x^2 + 2x^1 + 3x^0$$

$$\Rightarrow x^2 + 3x + 5 + x^2 + 4x + 4 = 3x^2 + 2x + 3$$

$$x^2 - 5x - 6 = 0$$

$$(x-6)(x+1) = 0 \quad (\text{Base cannot be negative})$$

Hence $x = 6$.

(OR)

As per the given number x must be greater than 5. Let consider $x = 6$

$$(135)_6 = (59)_{10}$$

$$(144)_6 = (64)_{10}$$

$$(323)_6 = (123)_{10}$$

$$(59)_{10} + (64)_{10} = (123)_{10}$$

So that $x = 6$

02. Ans: (a)

Sol: 8-bit representation of

$$+127_{10} = 01111111_{(2)}$$

1's complement representation of

$$-127 = 10000000.$$

2's complement representation of

$$-127 = 10000001.$$

No. of 1's in 2's complement of

$$-127 = m = 2$$

No. of 1's in 1's complement of

$$-127 = n = 1$$

$$\therefore m : n = 2 : 1$$

03. Ans: (c)

Sol: In 2's complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is 'X₃', hence it can be extended left any number of times.

04. Ans: (c)

Sol: Binary representation of $+(539)_{10}$:

2	539	
2	269 -1	
2	134 -1	
2	67 -0	
2	33 -1	
2	16 -1	
2	8 -0	
2	4 -0	
2	2 -0	
1	-0	

$$(+539)_{10} = (10000 11 0 11)_2 = (00100 0011011)_2$$

$$2'S \text{ complement} \rightarrow 110111100101$$

$$\text{Hexadecimal equivalent} \rightarrow (DE5)_H$$

05. Ans: 5

Sol: Symbols used in this equation are 0,1,2,3 Hence base or radix can be 4 or higher

$$(312)_x = (20)_x (13.1)_x$$

$$3x^2 + 1x + 2x^0 = (2x+0)(x+3x^0+x^{-1})$$

$$3x^2 + x + 2 = (2x) \left(x + 3 + \frac{1}{x} \right)$$

$$3x^2 + x + 2 = 2x^2 + 6x + 2$$

$$x^2 - 5x = 0$$

$$x(x-5) = 0$$

$$x = 0(\text{or}) x = 5$$

$$x \text{ must be } x > 3, \text{ So } x = 5$$



06. Ans: 3

Sol: $123_5 = x8_y$
 $1 \times 5^2 + 2 \times 5^1 + 3 \times 5^0 = x.y^1 + 8 \times y^0$
 $25 + 10 + 3 = xy + 8$
 $\therefore xy = 30$

Possible solutions:

- i. $x = 1, y = 30$
 - ii. $x = 2, y = 15$
 - iii. $x = 3, y = 10$
- $\therefore 3$ possible solutions exists.

07. Ans: 1

Sol: The range (or) distinct values

For 2's complement $\Rightarrow -(2^{n-1})$ to $+(2^{n-1}-1)$

For sign magnitude

$\Rightarrow -(2^{n-1}-1)$ to $+(2^{n-1}-1)$

Let $n = 2 \Rightarrow$ in 2's complement

$-(2^{2-1})$ to $+(2^{2-1}-1)$

-2 to $+1 \Rightarrow -2, -1, 0, +1 \Rightarrow X = 4$

$n = 2$ in sign magnitude $\Rightarrow -1$ to $+1 \Rightarrow Y = 3$

$X - Y = 1$

08. Ans: (c)

Sol: (a) $(68)_{16} = (001\ 101\ 000)_2$
 $= (1\ 5\ 0)_8$

(b) $(8C)_{16} = (010\ 001\ 100)_2$
 $= (2\ 1\ 4)_8$

(c) $(4F)_{16} = (001\ 001\ 111)_2$
 $= (1\ 1\ 7)_8$

(d) $(5D)_{16} = (001\ 011\ 101)_2$
 $= (1\ 3\ 5)_8$

09. Ans: (b)

Sol: A. $\begin{matrix} 7 & 5 \\ \downarrow & \downarrow \\ (111 & 101) \end{matrix}$ B. $\begin{matrix} 6 & 5 \\ \downarrow & \downarrow \\ (110 & 101) \end{matrix}$

C. $\begin{matrix} 3 & 7 \\ \downarrow & \downarrow \\ (011 & 111) \end{matrix}$ D. $\begin{matrix} 2 & 6 \\ \downarrow & \downarrow \\ (010 & 110) \end{matrix}$

10. Ans: (a)

Sol: 2's complement arithmetic is preferred in digital computers because it is efficient and one representation for zero.

11. Ans: (a)

Sol: $(11X1Y)_8 = (12C9)_{16}$

$8^4 + 8^3 + 64X + 8 + Y$

$= 16^3 + (2 \times 16^2) + (12 \times 16) + 9$

$4096 + 512 + 64X + 8 + Y$

$= 4096 + 512 + 192 + 9$

$\therefore 4616 + 64X + Y = 4809$

$64X + Y = 193$

By verification option (a) is correct

12. Ans: (d)

Sol: 2's comp no:

a_3	a_2	a_1	a_0
-------	-------	-------	-------

2's comp no. using 6 bits

\rightarrow

a_3	a_3	a_3	a_2	a_1	a_0
-------	-------	-------	-------	-------	-------

(2's comp no) $\times 2 + 1$

\rightarrow

a_3	a_3	a_2	a_1	a_0	1
-------	-------	-------	-------	-------	---

Chapter 2 Logic Gates & Boolean Algebra

01. Ans: (c)

Sol: Given 2's complement numbers of sign bits are x & y. z is the sign bit obtained by adding above two numbers. ∴ Overflow is indicated by $= \bar{x}\bar{y}z + xy\bar{z}$

Examples

1. A = +7 0111
 B = +7 0111
 14 1110 ⇒ $\bar{x}\bar{y}z$
2. A = +7 0111
 B = +5 0101
 12 1100 ⇒ $\bar{x}\bar{y}z$
3. A = -7 1001
 B = -7 1001
 -14 10010 ⇒ $xy\bar{z}$
4. A = -7 1001
 B = -5 1011
 -12 10100 ⇒ $xy\bar{z}$

02. Ans: (b)

Sol: Truth table of XOR

A	B	o/p
0	0	0
0	1	1
1	0	1
1	1	0

Stage 1:

Given one i/p = 1 Always.

1	X	o/p	
1	0	1	= \bar{X}
1	1	0	= X

For First XOR gate o/p = \bar{X}

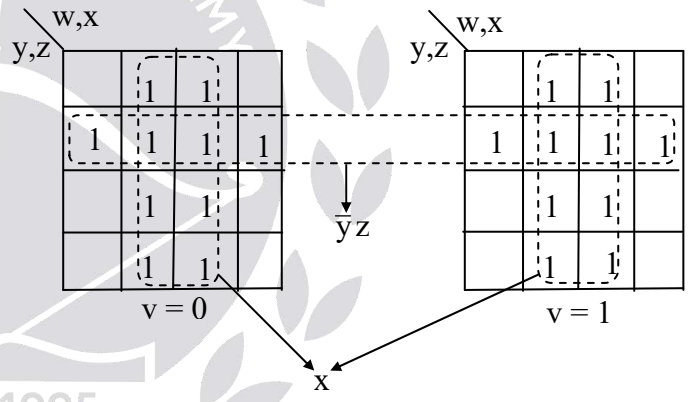
Stage 2:

\bar{X}	X	o/p	
0	1	1	
1	0	1	

For second XOR gate o/p = 1.
 Similarly for third XOR gate o/p = \bar{X} & for fourth o/p = 1
 For Even number of XOR gates o/p = 1
 For 20 XOR gates cascaded o/p = 1.

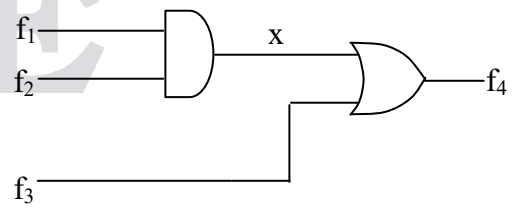
03. Ans: (b)

Sol:



04. Ans: (c)

Sol:

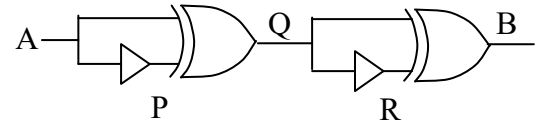


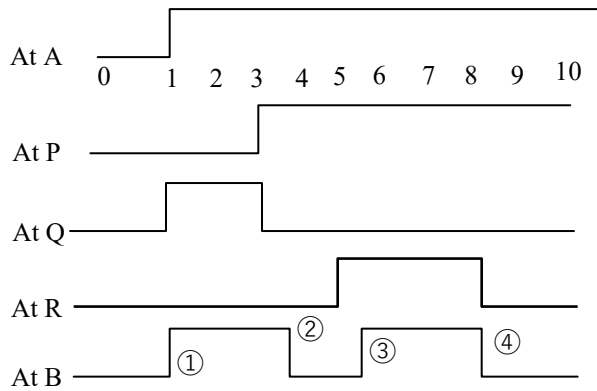
$$x = f_1 f_2$$

$$f_4 = f_1 \cdot f_2 + f_3$$

05. Ans: (d)

Sol:





06. Ans: (c)

Sol: $\overline{x_1} \oplus \overline{x_3} = \overline{x_1 x_3} + x_1 \overline{x_3} = y$

$\overline{x_2} \oplus \overline{x_4} = \overline{x_2 x_4} + x_2 \overline{x_4} = z$

$(\overline{x_1} \oplus \overline{x_3}) \oplus (\overline{x_2} \oplus \overline{x_4})$

$= y \oplus z = 0$, when $y = z$

\therefore option (c) is true

For all cases option A, B, D not satisfy.

07. Ans: (b)

Sol: $M(a,b,c) = ab + bc + ca$

$\overline{M(a,b,c)} = \overline{bc} + \overline{ab} + \overline{ac}$

$M(a, b, \overline{c}) = ab + b\overline{c} + \overline{c}a$

$M(\overline{M(a,b,c)}, M(a,b,\overline{c}), c)$

$= (\overline{bc} + \overline{ab} + \overline{ac})(ab + b\overline{c} + \overline{c}a)$
 $+ (ab + b\overline{c} + \overline{c}a)c + (\overline{bc} + \overline{ab} + \overline{ac})c$

$= (\overline{bc} + \overline{ab} + \overline{ac})(ab + b\overline{c} + \overline{c}a)$
 $+ (\overline{bc} + \overline{ab} + \overline{ac})c + abc$

$= \overline{ab}\overline{c} + \overline{ab}c + abc + \overline{ab}c$

$= \overline{c}[\overline{ab} + ab] + c[ab + \overline{ab}]$

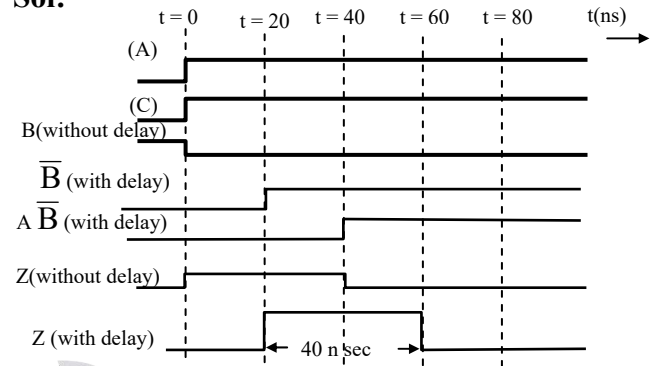
$= \sum m(1,2,4,7)$

$\therefore M(x, y, z) = a \oplus b \oplus c$

Where $x = \overline{M(a,b,c)}$, $y = M(a,b,\overline{c})$, $z = c$

08. Ans: 40

Sol:



\therefore Z is 1 for 40 nsec

09. Ans: (c)

Sol: Logic gates $\overline{X} + Y = \overline{X\overline{Y}} = \overline{XY_1}$

Where $Y_1 = \overline{Y}$

It is a NAND gate and thus the gate is 'Universal gate'.

10. Ans: (d)

Sol: A. $X = \overline{A} + \overline{B} = \overline{AB}$

B. $X = \overline{A} + B$

C. $X = \overline{\overline{A} + \overline{B}} = AB$

D. $X = \overline{\overline{A} \overline{B}} = A + B$

11. Ans: (a)

Sol: XOR gate is not a universal gate, because it is not possible to realize any Boolean function using only XOR gates.

12. Ans: (b)

Sol: (A) $A \oplus B = 0$ only when $A = B$

(B) $\overline{A} + \overline{B} = \overline{A \cdot B} = 0$ only when $A = 1$ and $B = 1$

(C) $\overline{A} \cdot B = 0$ only when $A = 1$ and $B = 0$

(D) $A \oplus B = 1$ only when $A \neq B$



13. Ans: (b)

Sol: (A) $ab + bc + ca + abc$

$$bc(1 + a) + ca + ab$$

$$bc + ca + ab$$

Inverse function $\overline{(ab + bc + ca)}$

$$= \bar{a}\bar{b} + \bar{b}\bar{c} + \bar{c}\bar{a}$$

(B) $ab + \bar{a}\bar{b} + \bar{c}$

Inverse function = $\overline{ab + \bar{a}\bar{b} + \bar{c}}$

$$= (\bar{a} + \bar{b})(a + b)c$$

$$= (\bar{a}b + a\bar{b})c$$

$$= (a \oplus b)c$$

(C) $(a+bc)$

Inverse function = $\overline{a + bc}$

$$= \bar{a}(\bar{b} + \bar{c})$$

(D) $(\bar{a} + \bar{b} + \bar{c})(a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + c)$

Inverse function

$$\overline{(\bar{a} + \bar{b} + \bar{c})(a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + c)}$$

$$= abc + \bar{a}bc + ab\bar{c}$$

14. Ans: (c)

Sol: AND gate : Boolean multiplication

OR gate : Boolean addition

NOT gate : Boolean complementation

15. Ans: (a)

Sol: When all inputs of a NAND-gate are shorted to get a one input, one output gate, it becomes an inverter.

When all inputs of a NAND – gate are at logic ‘0’ level, the output is at logic ‘1’ level.

Both statements are true and statement-II is the correct explanation of statement-I

16. Ans: (c)

Sol: A NAND gate represents a universal logic family.

Only two NAND gates are sufficient to accomplish any of the basic gates.

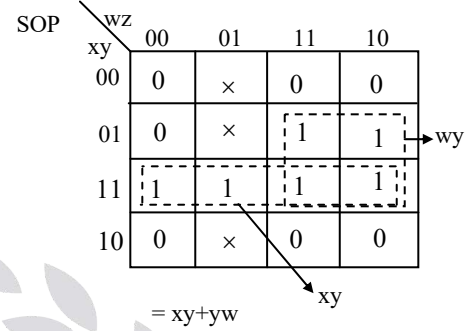
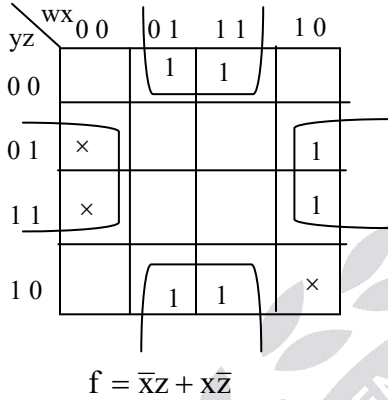
Statement-I is true but statement-II is false.

Chapter 3

K - Maps

01. Ans: (b)

Sol:

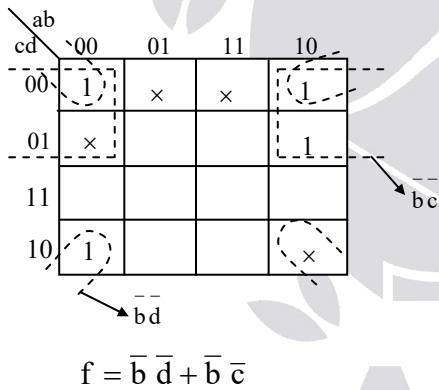


SOP: $x y + y w$

POS: $y(x + w)$

02. Ans: (b)

Sol:



04. Ans: (a)

Sol: For n-variable Boolean expression,

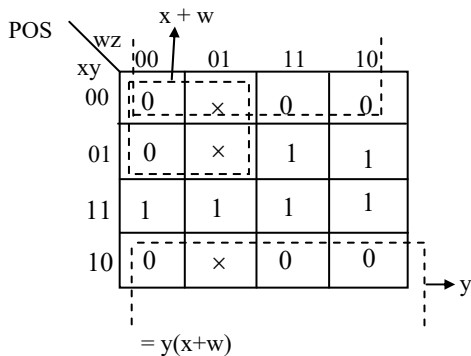
Maximum number of minterms = 2^n

Maximum number of implicants = 2^n

Maximum number of prime implicants = $\frac{2^n}{2}$
 $= 2^{n-1}$

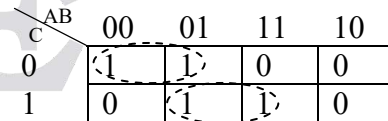
03.

Sol:



05. Ans: (c)

Sol:



$F(A, B, C) = \bar{A}\bar{C} + BC$

06. Ans: 1

Sol: After minimization = $(\overline{A + B + C + D})$
 $= ABCD$

∴ only one minterm.



07. Ans: 3

Sol: $\bar{w}\bar{z} + \bar{w}xy + \bar{x}y\bar{z}$

	yz			
wx	00	01	11	10
00	1			1
01	1	1		1
11				
10				1

08. Ans: (c)

Sol: Given K-map is

	X_1X_2			
X_3X_4	00	01	11	10
00	1		d	d
01		1	d	1
11		d	1	
10	1	d		d

$$\text{Output} = \bar{X}_2 \bar{X}_4 + X_1 \bar{X}_3 + X_2 X_4$$

09. Ans: None

Sol:

	x	
yz	0	1
00	1	1
01	1	
11	1	1
10	1	1

The minimal form is

$$F = \bar{x} + y + \bar{z}$$

None of the options is correct

10. Ans: (a)

Sol: Given K-map

	AB			
CD	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

No. of essential prime implicants = 4.

4

Combinational Circuits

Chapter

01. Ans: (d)

Sol: Let the output of first MUX is "F₁"

$$F_1 = AI_0 + \bar{A}I_1$$

Where A is selection line, I₀, I₁ = MUX Inputs

$$F_1 = \bar{S}_1 \cdot W + S_1 \cdot \bar{W} = S_1 \oplus W$$

Output of second MUX is

$$F = \bar{A} \cdot I_0 + A \cdot I_1$$

$$F = \bar{S}_2 \cdot F_1 + S_2 \cdot \bar{F}_1$$

$$F = S_2 \oplus F_1$$

$$\text{But } F_1 = S_1 \oplus W$$

$$F = S_2 \oplus S_1 \oplus W$$

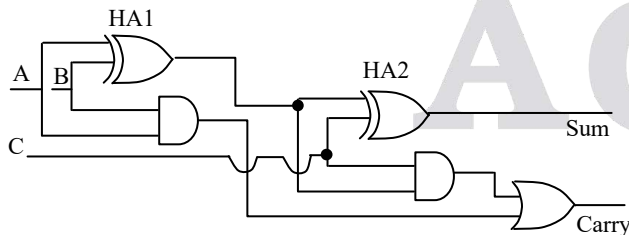
$$\text{i.e., } F = W \oplus S_1 \oplus S_2$$

02. Ans: 19.2

Sol: One AND/OR gate delay = 1.2 μs

One XOR gate delay = 2.4 μs

Full Adder with 2 Half Adder



In one F.A; Sum delay = 4.8 μs

Carry delay = 2.4 + 1.2 + 1.2 μs = 4.8 μs

∴ RippleCarry waiting time
= 4.8 × 3 = 14.4 μs

Final Result time = 14.4 + 4.8 = 19.2 μsec

03. Ans: (a)

Sol: The given circuit is binary parallel adder/subtractor circuit. It performs A+B, A-B but not A + 1 operations.

K	C ₀	Operation
0	0	A+B (addition)
0	1	A+B+1 (addition with carry)
1	0	A+ \bar{B} (1's complement addition)
1	1	A+ \bar{B} +1 (2's complement subtraction)

04. Ans: (d)

Sol: It is expansion of 2:4 decoders to 1:8 demultiplexer A₁, A₀ must be connected to S₁, S₀ i.e., R = S₀, S = S₁
Q must be connected to S₂ i.e., Q = S₂
P is serial input must be connected to D_{in}

05. Ans: 6

Sol: T = 0 → NOR → MUX 1 → MUX 2
2ns 1.5ns 1.5ns

Delay = 2ns + 1.5ns + 1.5ns = 5ns

T = 1 → NOT → MUX 1 → NOR → MUX 2
1ns 1.5ns 2ns 1.5ns

Delay = 1ns + 1.5ns + 2ns + 1.5ns = 6ns

Hence, the maximum delay of the circuit is 6ns

06. Ans: -1

Sol: When all bits in 'B' register is '1', then only it gives highest delay.

∴ '-1' in 8 bit notation of 2's complement is 1111 1111

07. Ans: (d)

Sol: The race hazard problem does not occur in combinational circuits.

The output of a combinational circuit depends upon present inputs only.

Statement-I is false but Statement-II is true.

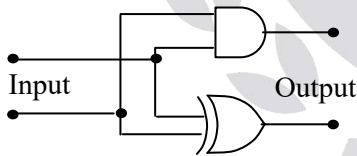
08. Ans: (b)

Sol: A de-multiplexer can be used as a decoder. A decoder with enable input acts as a demultiplexer, while using Enable input as a data input line. De-multiplexer is realized using AND gates.

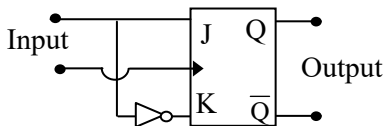
A	B	F
0	0	C
0	1	C
1	0	\bar{C}
1	1	\bar{C}

09. Ans: (b)

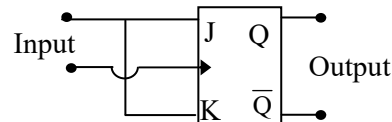
Sol: Half Adder



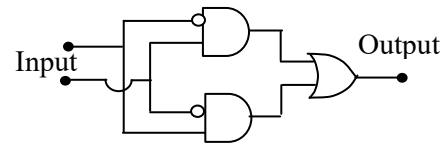
D-Flipflop



T-Flipflop

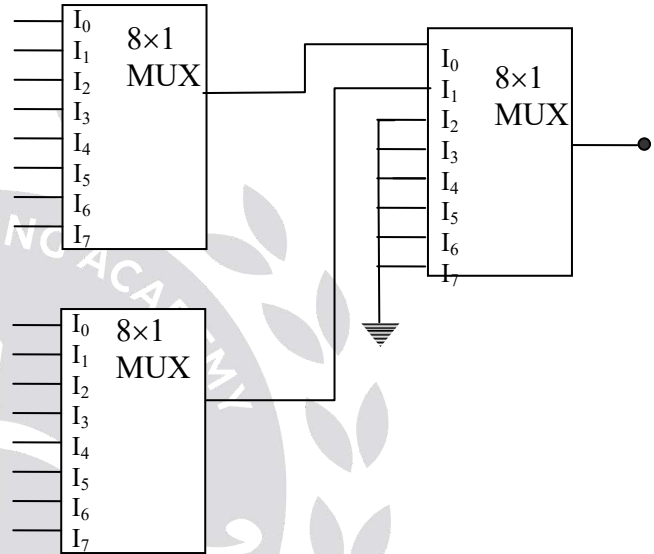


Exclusive - OR



10. Ans: (b)

Sol: →A 64 input MUX using 8-input MUX



→A 6-variable function can be implemented using 6-input MUX

11. Ans: 195

Sol: In a 16 bit parallel binary adder, the carry has to propagate 15 stages plus the maximum of time taken for producing sum and carry worst case Delay, $T = 15 \times 12 + 15$

$$T = 180 + 15$$

$$T = 195 \text{ ns}$$

12. Ans: (b)

Sol: Any Boolean function can be realized by using a suitable multiplexer.

A multiplexer can be realized using NAND and NOR gates, which are universal gates.

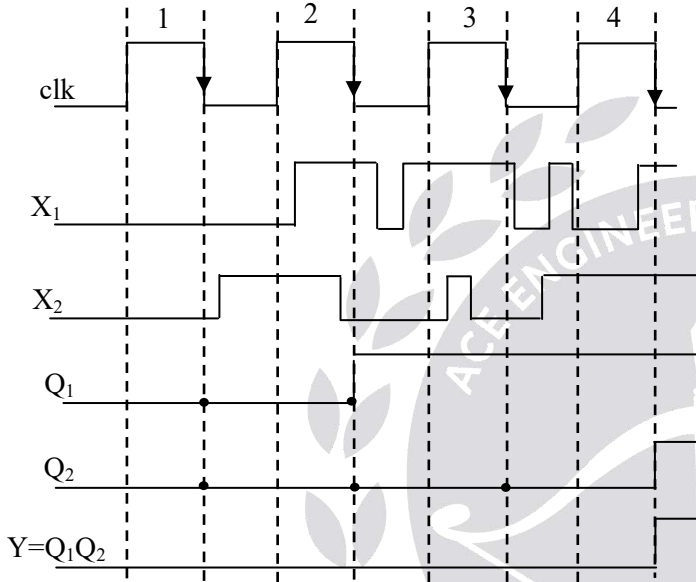
Both statements are correct but statement-II is not a correct explanation for statement-I.

01. Ans: (c)

Sol: Given Clk, X_1 , X_2

Output of First D-FF is Q_1

Output of Second D-FF is Q_2



02. Ans: 4

Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

03. Ans: 7

Sol: The counter is cleared when

$$Q_D Q_C Q_B Q_A = 0110$$

Clk	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	0	0

As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get's cleared during the 7th clock pulse.

$$\therefore \text{mod of counter} = 7$$

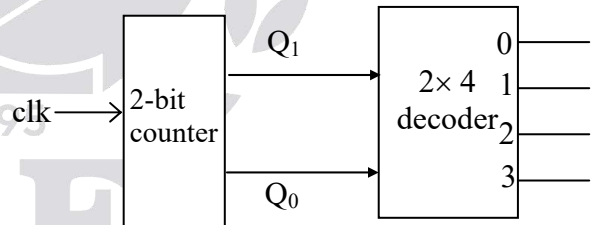
04. Ans: (b)

Sol: The given circuit is a mod 4 ripple down counter. Q_1 is coming to 1 after the delay of $2\Delta t$.

CLK	Q_1	Q_0
	0	0
1	1	1
2	1	0
3	0	1
4	0	0

05. Ans: (c)

Sol: Assume $n = 2$



Outputs of counter is connected to inputs of decoder

Counter outputs		Decoder inputs		Decoder outputs			
Q_1	Q_0	a	b	d_3	d_2	d_1	d_0
0	0	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0

The overall circuit acts as 4-bit ring counter $n = 2$

$$\therefore k = 2^2 = 4, \text{ k-bit ring counter}$$



06. Ans: (b)

Sol:

CLK	Serial in= $B \oplus C \oplus D$	A B C D
0		1 0 1 0
1	1 →	1 1 0 1
2	0 →	0 1 1 0
3	0 →	0 0 1 1
4	0 →	0 0 0 1
5	1 →	1 0 0 0
6	0 →	0 1 0 0
7	1 →	1 0 1 0

∴ After 7 clock pulses content of shift register become 1010 again

07. Ans: (b)

Sol:

J	K	Q	\bar{Q}_n	$T = (J + Q_n)(K + \bar{Q}_n)$	Q_{n+1}
0	0	0	1	$0.1 = 0$	0
0	0	1	0	$1.0 = 0$	1
0	1	0	1	$0.1 = 0$	0
0	1	1	0	$1.1 = 1$	0
1	0	0	1	$1.1 = 1$	1
1	0	1	0	$1.0 = 0$	1
1	1	0	1	$1.1 = 1$	1
1	1	1	0	$1.1 = 1$	0

J	KQ_n	00	01	11	10
0				1	
1		1		1	1

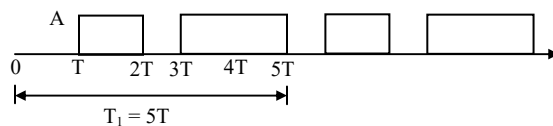
$$T = J \bar{Q}_n + KQ_n = (J + Q_n)(K + \bar{Q}_n)$$

08. Ans: 1.5

Sol:

Clk	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Y = Q ₃ + Q ₅
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0

The waveform at OR gate output, Y is [A = +5V]



Average power

$$P = \frac{V_{Ao}^2}{R} = \frac{1}{R} \left[\frac{1}{T_1} \int_0^{T_1} y^2(t) dt \right] = \frac{1}{RT_1} \left[\int_T^{2T} A^2 dt + \int_{3T}^{5T} A^2 dt \right]$$

$$= \frac{A^2}{RT_1} [(2T - T) + (5T - 3T)] = \frac{A^2 \cdot 3T}{R(5T)} = \frac{5^2 \cdot 3}{10 \times 5} = 1.5 \text{ mw}$$



09. Ans: (b)

Sol:

Present State	Next State		Output (Y)	
	X = 0	X = 1	X = 0	X = 1
A	A	E	0	0
B	C	A	1	0
C	B	A	1	0
D	A	B	0	1
E	A	C	0	1

Step (1):

By replacing state B as state C then state B, C are equal.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
B	B	A
D	A	B
E	A	B

Step (2):

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
D	A	B
E	A	B

State D, E are equal, remove state E and replace E with D in next state.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B
D	A	B

Finally reduced state table is

Reduced state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B

∴ 3 states are present in the reduced state table

10. Ans: (c)

Sol: State table for the given state diagram

State	Input	Output
S ₀	0	1
S ₀	1	0
S ₁	0	1
S ₁	1	0

Output is 1's complement of input.

11. Ans: (c)

Sol: In state (C), when XYZ = 111, then Ambiguity occurs

Because, from state (C)

⇒ When X = 1, Z = 1

⇒ N.S is (A)

When Y = 1, Z = 1 ⇒ N.S is (B)



12. Ans: (c)

Sol: For Asynchronous sequential circuits clock is applied at one flip flop and the next stage receives clock from previous stage output.

13. Ans: (d)

Sol: Master slave JK flip flop is a edge triggered flip flop.

14. Ans: (b)

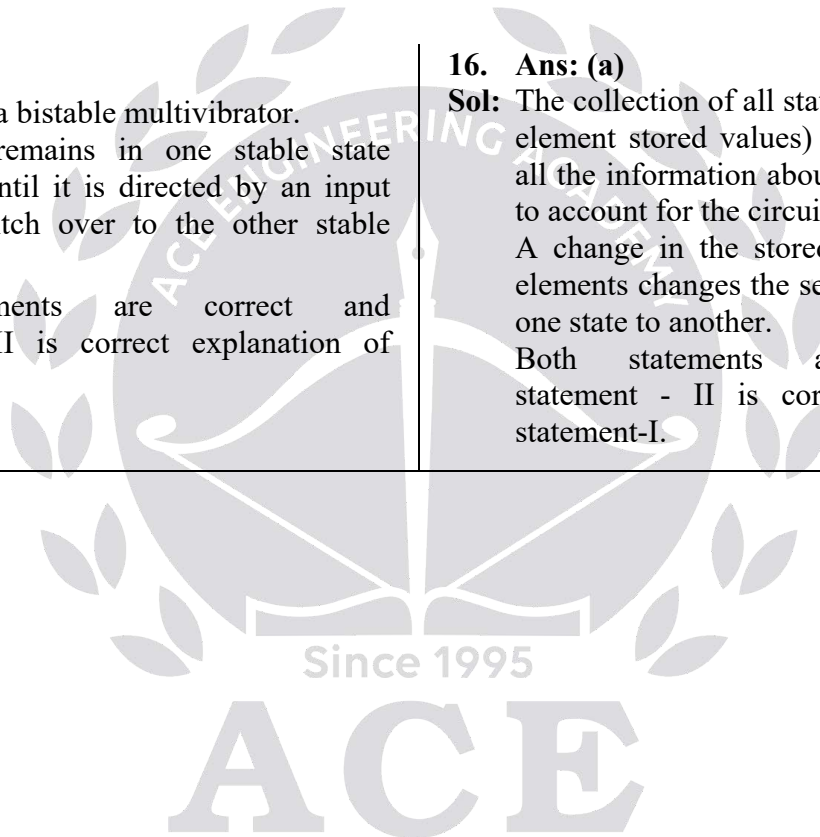
Sol: Divider : Bi stable multivibrator
Clips input voltage at Two predetermined levels : Schmitt trigger
Square wave generator : Astable multivibrator
Narrow current pulse generator : Blocking oscillator

15. Ans: (a)

Sol: A flip-flop is a bistable multivibrator. A flip-flop remains in one stable state indefinitely until it is directed by an input signal to switch over to the other stable state.
Both statements are correct and statement - II is correct explanation of statement-I

16. Ans: (a)

Sol: The collection of all state variables (memory element stored values) at any time, contain all the information about the past, necessary to account for the circuit's future behaviour. A change in the stored values in memory elements changes the sequential circuit from one state to another.
Both statements are correct and statement - II is correct explanation of statement-I.



6

Logic Gate Families

Chapter

01. Ans: (b)

Sol: $V_{OH}(\min)$:-

(High level output voltage)

The minimum voltage level at a Logic circuit output in the logic '1' state under defined load conditions.

$V_{OL}(\max)$:-

(Low level output voltage)

The maximum voltage level at a logic circuit output in the Logical '0' state under defined load conditions.

$V_{IL}(\max)$:- (Low level input voltage)

The maximum voltage level required for a logic '0' at an input. Any voltage above this level will not be accepted as a Low by the logic circuit.

$V_{IH}(\min)$:- (High level Input voltage)

The minimum voltage level required for logic '1' at an input. Any voltage below this level will not be accepted as a HIGH by the Logic circuit.

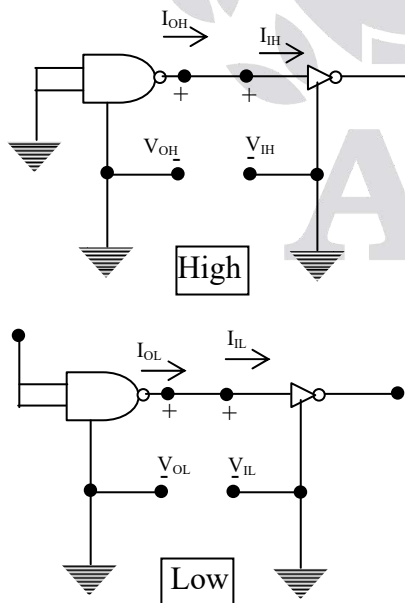


Fig: currents and voltages in the two logic states.

02. Ans: (b)

Sol: Fan out is minimum in DTL

(High Fan-out = CMOS)

Power consumption is minimum in CMOS.
Propagation delay is minimum in ECL
(fastest = ECL)

03. Ans: (b)

Sol: When $V_1 = 2.5V$,

Q_1 is in reverse active region

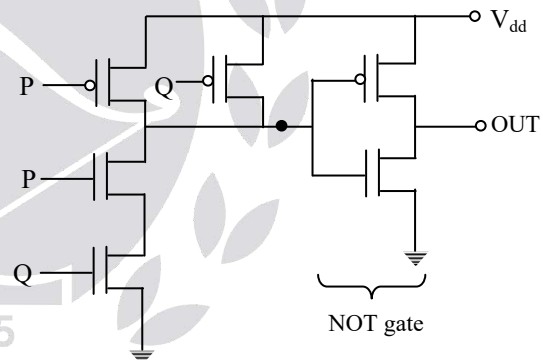
Q_2 is in saturation region

Q_3 is in saturation region

Q_4 is in cut-off region

04. Ans: (d)

Sol: The given circuit can be redrawn as below:



$$\text{OUT} = \overline{(\overline{PQ})} = PQ$$

$$= P \text{ AND } Q$$

05. Ans: (b)

Sol: As per the description of the question, when the transistor Q_1 and diode both are OFF then only output $z = 1$.

X	Y	Z	Remarks
0	0	0	Q_1 is OFF, Diode is ON
0	1	1	Q_1 is OFF, Diode is OFF
1	0	0	Q_1 is ON, Diode is OFF
1	1	0	Q_1 is ON, Diode is OFF

$$\text{Hence } Z = \overline{XY}$$



06. Ans: (c)

Sol: Propagation delay time is less in Schottky transistor because it is not entering in to saturation region. Schottky transistors operate in active region whenever it is ON.

07. Ans: (b)

Sol: To obtain high Switching speed BJT operated in active region. In the active region BJT works as a linear element.

08. Ans: (a)

Sol: When transistor switches are to be used in an application where speed is a premium, it is better to reduce the storage time.

It is comparatively easy to reduce storage time rather than the rise time and fall time of a transistor switch.

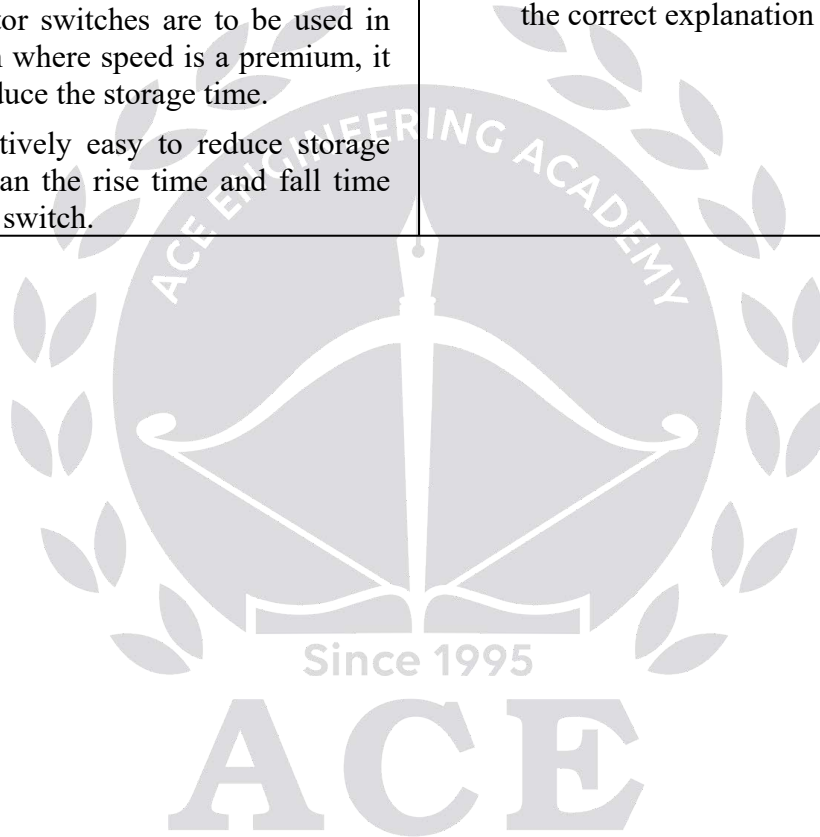
Both statements are true and statement-II is the correct explanation of statement-I.

09. Ans: (a)

Sol: The TTL NAND gate in tri-state output configuration can be used for a bus arrangement with more than one gate output connected to a common line.

The tri-state configuration has a control input, which control the bus line.

Both statements are true and statement-II is the correct explanation of statement-I.



Chapter 7

Semiconductor Memories

01. Ans: (b)

Sol: Square of a 4 - bit number can be at most 8 - bit number.

{ i.e $(1111)_2 = (15)_{10}$
 $[(15)_{10}]^2 = (225)_{10}$ }.

Therefore ROM requires 8 data lines.

Data is with size of 4 bits
 ROM must require 4 address lines and 8 data lines

ROM = $2^n \times m$

n = inputs (address lines),

m = output lines

n = 4, m = 8.

02. Ans: (a)

Sol: ROM is used to design a combinational circuit. The number of address lines of the ROM is equal to the number of input variables in the truth table.

ROM is represented as $2^n \times m$ where 2^n inputs and m output lines.

[Where n = address bits]

03. Ans: (b)

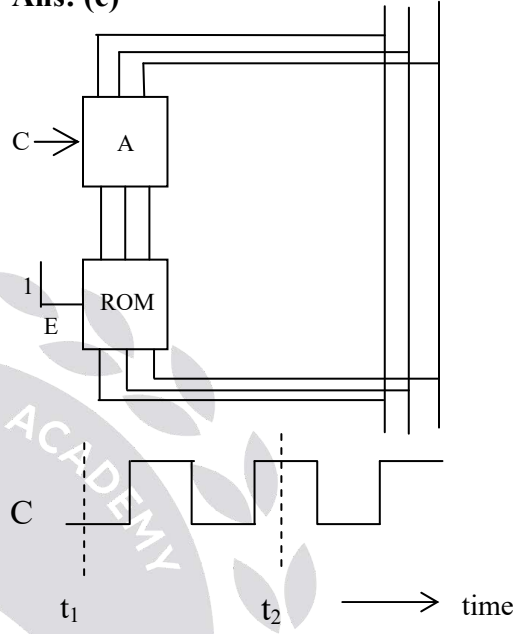
Sol:

i/p s				o/p s				2421 Outputs
X ₃	X ₂	X ₁	X ₀	Y ₃	Y ₂	Y ₁	Y ₀	
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	3
0	1	0	0	0	1	0	0	4
0	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	6
0	1	1	1	1	1	0	1	7
1	0	0	0	1	1	1	0	8
1	0	0	1	1	1	1	1	9
1	0	1	0	x	x	x	x	
1	0	1	1	x	x	x	x	
1	1	0	0	x	x	x	x	
1	1	0	1	x	x	x	x	
1	1	1	0	x	x	x	x	
1	1	1	1	x	x	x	x	

The outputs are in 2 4 2 1 BCD number

04. Ans: (c)

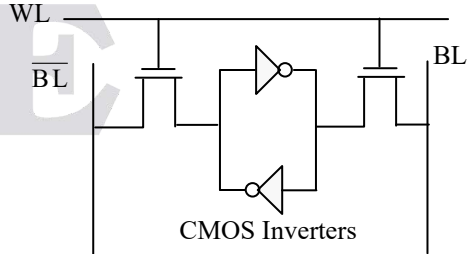
Sol:



At the rising edge of the First clock pulse the content of location $(0110)_2 = 6 \Rightarrow 1010$ appears on the data bus, at the rising of the second clock pulse the content of location $(1010)_2 = 10_2 \Rightarrow 1000$ appears on the data bus.

05. Ans: (b)

Sol: 1-bit SRAM memory cell is



In 2 Inverters, output of the 1st Inverter is connected to Gate Input of 2nd Inverter and vice versa.

06. Ans: (c)

Sol: SRAM is relatively high speed memory that stores the most recently used instructions
 \therefore It is preferred when the requirement is of lower access time.



07. Ans: (b)

Sol: SRAM : This contains conventional storage like latches (BJT or MOSFET) and has both Read and Write operation.

ROM : This contains conventional storage like latches (BJT or MOSFET) and it is non volatile.

PLA : This contains a set of AND, OR and INVERT logic gates and can be programmed.

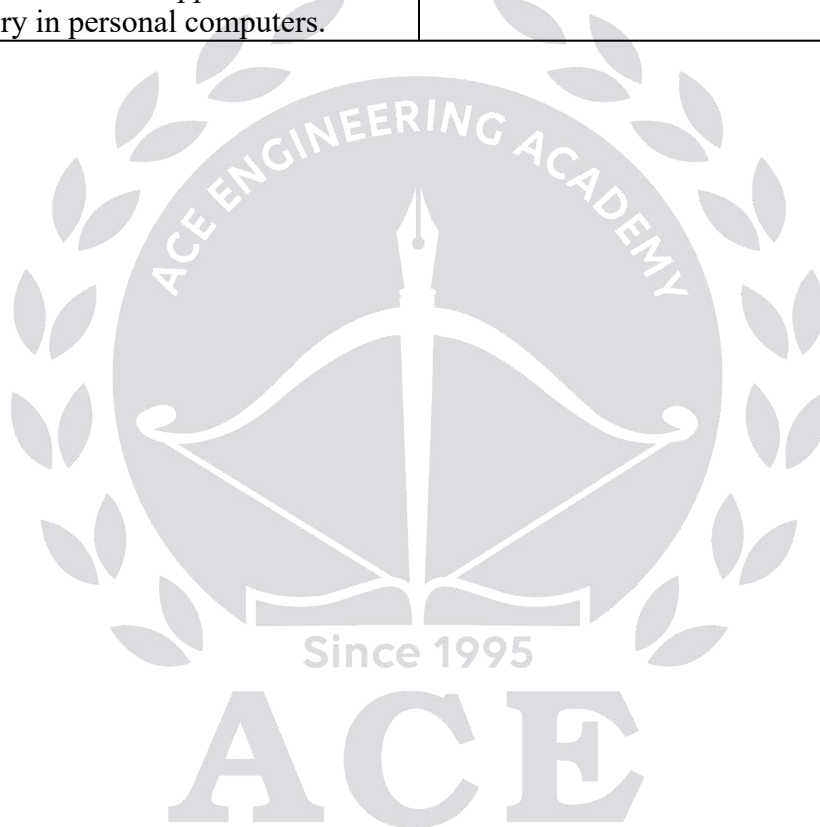
DRAM : This contains only MOSFET's and needs periodic refreshing.

08. Ans: (d)

Sol: SRAM is more expensive and less dense than DRAM and is therefore not used for high capacity, low - cost applications such as main memory in personal computers.

09. Ans: (a)

Sol: In DRAM the bit is stored as a charge in capacitor, and it is made up of MOS transistors.



8

A/D & D/A Converters

Chapter

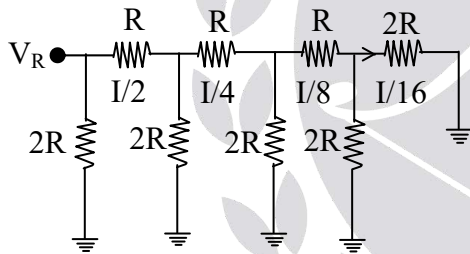
01. Ans: (b)

Sol:

CLK	Counter			Decoder				V ₀
	Q ₂	Q ₁	Q ₀	D ₃	D ₂	D ₁	D ₀	
1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1	1
3	0	1	0	0	0	1	0	2
4	0	1	1	0	0	1	1	3
5	1	0	0	1	0	0	0	8
6	1	0	1	1	0	0	1	9
7	1	1	0	1	0	1	0	10
8	1	1	1	1	0	1	1	11

02. Ans: (b)

Sol:



$$R_{\text{equ}} = (((((2R \parallel 2R) + R) \parallel 2R) + R) \parallel 2R) + R \parallel 2R$$

$$R_{\text{equ}} = R = 10\text{k}\Omega.$$

$$I = \frac{V_R}{R} = \frac{10\text{V}}{10\text{k}} = 1\text{mA}.$$

$$\begin{aligned} \text{Current division at } \frac{I}{16} \\ = \frac{1 \times 10^{-3}}{16} = 62.5 \mu\text{A} \end{aligned}$$

03. Ans: (c)

Sol: Net current at inverting terminal,

$$I_i = \frac{I}{4} + \frac{I}{16} = \frac{5I}{16}$$

$$\begin{aligned} V_0 &= -I_i R = -\frac{5I}{16} \times 10\text{k}\Omega \\ &= \frac{-5 \times 1 \times 10^{-3} \times 10 \times 10^3}{16} = -3.125\text{V} \end{aligned}$$

04. Ans: (d)

Sol: Given that $V_{\text{DAC}} = \sum_{n=0}^3 2^{n-1} b_n$ Volts

$$V_{\text{DAC}} = 2^{-1} b_0 + 2^0 b_1 + 2^1 b_2 + 2^2 b_3$$

$$\Rightarrow V_{\text{DAC}} = 0.5b_0 + b_1 + 2b_2 + 4b_3$$

Initially counter is in 0000 state

Up counter o/p	V _{DAC} (V)	o/p of comparator
0 0 0 0	0	1
0 0 0 1	0.5	1
0 0 1 0	1	1
0 0 1 1	1.5	1
0 1 0 0	2	1
0 1 0 1	2.5	1
0 1 1 0	3	1
0 1 1 1	3.5	1
1 0 0 0	4	1
1 0 0 1	4.5	1
1 0 1 0	5	1
1 0 1 1	5.5	1
1 1 0 0	6	1
1 1 0 1	6.5	0

When $V_{\text{DAC}} = 6.5$ V, the o/p of comparator is '0'. At this instant, the clock pulses to the counter are stopped and the counter remains in 1101 state.

\therefore The stable reading of the LED display is 13.



05. Ans: (b)

Sol: The magnitude of error between V_{DAC} & V_{in} at steady state is $|V_{DAC} - V_{in}| = |6.5 - 6.2| = 0.3 \text{ V}$

06. Ans: (a)

Sol: In Dual slope

$$ADC \Rightarrow V_{in} T_1 = V_R \cdot T_2$$

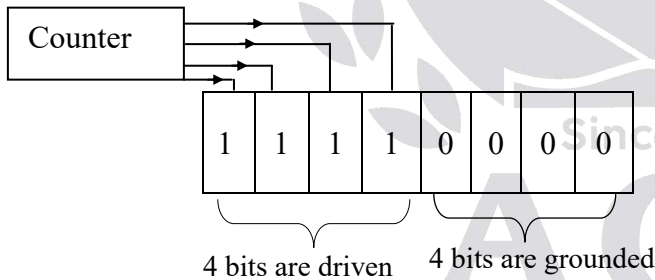
$$\Rightarrow V_{in} = \frac{V_R T_2}{T_1} = \frac{100 \text{ mV} \times 370.2 \text{ ms}}{300 \text{ ms}}$$

DVM indicates = 123.4

07. Ans: (d)

Sol: No. of bits = 8,

Reference voltage = 8V



Maximum peak to peak amplitude of the waveform at the output of the digital to analog converter is

$$V_{\max} = \frac{V_{\text{ref}}}{2^n} (d_n 2^n) = \frac{8}{256} \times 240 = 7.5 \text{ V}$$

08. Ans: (d)

Sol: Ex: $f_{in} = 1 \text{ kHz} \rightarrow f_s = 2 \text{ kHz}$

$$f_{in} = 25 \text{ kHz} \leftarrow f_s = 50 \text{ kHz}$$

$$1. \text{ Max conversion time} = 2^{N+1} T = 2^{11} \cdot 1 \mu\text{s} = 2048 \mu\text{s}$$

$$2. \text{ Sampling period} = T_s \geq \text{maximum conversion time}$$

$$T_s \geq 2048 \mu\text{s}$$

$$3. \text{ Sampling rate } f_s = \frac{1}{T_s} \leq \frac{1}{2048 \times 10^{-6}}$$

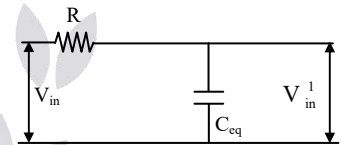
$$f_s \leq 488 \quad f_s \leq 500 \text{ Hz}$$

$$4. f_{in} = \frac{f_s}{2} = 250 \text{ Hz}$$

09. Ans: (b)

Sol:

$$V_{in}^1 = \frac{V_{in} \cdot T}{RC_{eq}}$$



V_{in}^1 has to settle down within $\frac{1}{2}$ LSB of full scale value.

$$\text{i.e. } \frac{509}{510} V_{in} = \frac{V_{in} \cdot T}{75 \times (255 \times 8 \times 10^{-12})}$$

$$\Rightarrow T = (75 \times 255 \times 8 \times 10^{-12}) \times \frac{509}{510}$$

$$T \approx 0.15 \mu\text{sec}$$

Thus sample period $T_s \geq T$

$$T_s \geq 0.15 \text{ m sec}$$

$$f_s \text{ max} = \frac{1}{T_{s, \text{min}}}$$

$$= \frac{1}{0.15 \times 10^{-6}} \text{ Hz}$$

$$\approx 6 \text{ Megasamples}$$



10. Ans: (a)

Sol: Dual-slope A/D converter is the most preferred A/D conversion approach in digital multimeters.

Dual-slope A/D converter provides high accuracy in A/D conversion, while at the same time suppressing the hum effect on the input signal.

Both Statements are true and statement-II is the correct explanation of statement-I.

11. Ans: (d)

Sol: SAR type ADC : Settling time for n-bits is $(n+2) T$ clock pulses

Flash ADC : $(2^n - 1)$ comparators required for n-bit dual

Dual slope ADC : Works well even in noisy environment

Counter DAD : Settling time dependent on the input

12. Ans: (c)

Sol: Dual slope ADC : Hum rejection approximation

Counter-ramp ADC : Conversion time dependent on single amplitude

Successive ADC : Fixed conversion time, depends on the number of bits

Simultaneous ADC: High speed operation

13. Ans: (a)

Sol: The output of an 8-bit A to D converter is 40H for an input of 2.5V.

ADC has an output range of 00 to FFH for an input range of $-5V$ to $+5V$.

Both Statements are true and statement-II is the correct explanation of statement-I.

14. Ans: (c)

Sol: Digital ramp converter is the slowest ADC. Conversion time for digital ramp ADC is not N^2T .

15. Ans: (b)

Sol: Resolution for n-bit A/D converter in percentage.

$$= \frac{1}{2^n - 1} \times 100$$

$$= \frac{1}{2^{12} - 1} \times 100$$

$$= 2.443 \times 10^{-4} \times 100$$

$$= 0.02441$$

01. Ans: (a)

Sol: chip select is an active low signal for $\text{chipselect} = 0$; the inputs for NAND gate must be let us see all possible cases for $\text{chipselect} = 0$ condition

A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
0	0	0	0	0	0	X	X
0	0	1	1	0	0	X	X
0	1	0	1	0	0	X	X
0	1	1	0	0	0	X	X
1	0	0	1	0	0	X	X
1	0	1	0	0	0	X	X
0	0	0	0	1	1	X	X
0	0	1	1	1	1	X	X
0	1	0	1	0	0	X	X
0	1	1	0	0	0	X	X
1	0	0	1	0	0	X	X
1	0	0	0	0	0	X	X

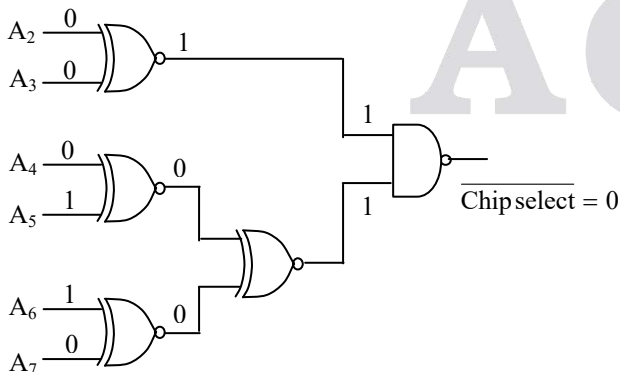
$\rightarrow 60H (A_1A_0=00)$

$\rightarrow 63H (A_1A_0=11)$

The only option that suits here is option(a)

A₀ & A₁ are used for line selection

A₂ to A₇ are used for chip selection



∴ Address space is 60H to 63H

A₀ to A₁₁ are used for line selection

A₁₂ to A₁₅ are used for chip selection

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁ -----A ₀
1	1	1	0	0-----0 =E000H
1	1	1	0	1-----1 =EFFFH

02. Ans: (d)

Sol:

- Both the chips have active high chip select inputs.
- Chip 1 is selected when A₈ = 1, A₉ = 0
- Chip 2 is selected when A₈ = 0, A₉ = 1
- Chips are not selected for combination of 00 & 11 of A₈ & A₉
- Upon observing A₈ & A₉ of given address Ranges, F800 to F9FF is not represented

03. Ans: (d)

Sol: The I/O device is interfaced using “Memory Mapped I/O” technique.

The address of the Input device is

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0

=F8F8_H

The Instruction for correct data transfer is = LDA F8F8H

04. Ans: (b)

Sol:

- Out put 2 of 3×8 Decoder is used for selecting the output port. ∴ Select code is 010

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	---	A ₀
0	1	0	1	0	0	---	0

⇒ 5000H

- This mapping is memory mapped I/O



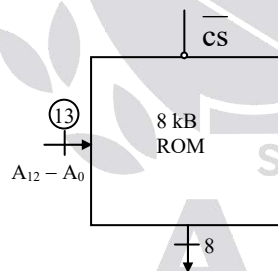
05. Ans: (d)

Sol:

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉ ----	A ₀	
0	0	0	0	1	0	0	----	0 =0800H
			⋮					⋮
0	0	0	0	1	0	1	----	1 =0BFFH
			⋮					⋮
0	0	0	1	1	0	0	----	0 =1800H
			⋮					⋮
0	0	0	1	1	0	1	----	1 =1BFFH
			⋮					⋮
0	0	1	0	1	0	0	----	0 =2800H
			⋮					⋮
0	0	1	0	1	0	1	----	1 =2BFFH
			⋮					⋮
0	0	1	1	1	0	0	----	0 =3800H
			⋮					⋮
0	0	1	1	1	0	1	----	1 =3BFFH

06. Ans: (a)

Sol: Address Range given is



	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
1000H →	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2FFFH →	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1

To provide \overline{CS} as low, The condition is

$$A_{15} = A_{14} = 0 \text{ and } A_{13} A_{12} = 01 \text{ (or) } (10)$$

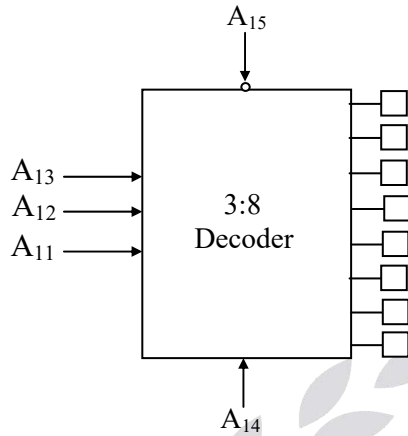
i.e $A_{15} = A_{14} = 0$ and $A_{13} A_{12}$ shouldn't be 00, 11.

$$\text{Thus it is } A_{15} + A_{14} + [A_{13}A_{12} + \overline{A_{13}}\overline{A_{12}}]$$



07. Ans: (a)

Sol:



A₁₅, A₁₄ are used for chip selection

A₁₃, A₁₂, A₁₁ are used for input of decoder

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀ ----- A ₀
Enable of decoder		Input of decoder			Address of chip

Size of each memory block = $2^{11} = 2K$

08. Ans: (a)

Sol: The data path contains all the circuits to process data within the CPU with the help of which data is suitably transformed.

It is the responsibility of the control path to generate control and timing signals as required by the opcode.

Both Statements are true and statement-II is the correct explanation of statement-I.

09. Ans: (b)

Sol: Program counter is a register that contains the address of the next instruction to be executed.

IR (Instruction Register) is not accessible to programmer.

Both Statements are true but statement-II is not correct explanation of statement-I.

10. Ans: (a)

Sol: A processor can reference a memory stack without specifying an address.

The address is always available and automatically updated in the stack pointer.

Both Statements are true and statement-II is the correct explanation of statement-I.

11. Ans: (c)

Sol: The programmer has to initialize the stack pointer based on design requirements.

12. Ans: (b)

Sol: The DMA technique is more efficient than the Interrupt-driven technique for high volume I/O data transfer.

The DMA technique does not make use of the Interrupt mechanism.

Both Statements are true but statement-II is not correct explanation of statement-I.



13. Ans: (c)

Sol: A microcontroller has onchip (inbuilt) memory, where as a microprocessor has no such internal memory.

The program to be run by microprocessor is to be store in separate memory (E²PROM) chip and to be interfaced microprocessor.

14. Ans: (d)

Sol: INTR is a non vectored interrupt. As such external hardware is required to supply vector address. SIM is not used with respect to INTR. The SIM is used for selective local masking of three hardware maskable vectored interrupts (RST 7.5, RST 6.5, RST 5.5)



01. Ans: (c)

Sol:

6010H : LXI H,8A79H ; (HL) = 8A79H

6013H : MOV A, L ; (A)←(L) = 79

6014H : ADD H ; (A) = 0111 1001

+

; (H) = 1000 1010

; (A) = 0000 0011

CY = 1, AC = 1

6015H : DAA ; 66 Added to (A)

since CY=1 &

AC=1

; (A) = 69H

6016H : MOV H,A ; (H)←(A) = 69H

6017H : PCHL ; (PC)←(HL) = 6979H

02. Ans: (c)

Sol: 0100H : LXI SP, 00FFH ; (SP) = 00FFH

0103H : LXI H, 0107 H ; (HL) = 0107H

0106H : MVI A, 20H ; (A) = 20H

0108H : SUB M ; (A)←(A)-(0107)

; (0107) = 20H

; (A) = 00H

The contents of Accumulator is 00H

03. Ans: (c)

Sol: LXI SP, 00FFH ; (SP) = 00FFH

LXI H, 0107 H ; (HL) = 0107H

MVI A, 20H ; (A) = 20H

SUB M ; (A)←(A) - (0107)

; (0107) = 20H = M

; (A) = 00H

ORI 40H ; A ∨ 40H

A = 40H

ADD M ; 40H + 20H = 60H

04. Ans: (c)

Sol: SUB1 : MVI A, 00H A← 00H

CALL SUB2 → program will shifted to
SUB 2 address location

SUB 2 : INR A → A

01H

RET → returned to the main program

∴ The contents of Accumulator after
execution of the above SUB2 is 02H

05. Ans: (c)

Sol: The loop will be executed until the value in
register equals to zero, then,

Execution time

= 9(7T+4T+4T+10T)+(7T+4T+4T+7T)+7T

= 254T

06. Ans: (d)

Sol: H=255 : L = 255, 254, 253, ----0

H=254 : L = 0, 255, 254, -----0

|

H=1 : L = 0,255,254,253,---0

H=0 : —

→ In first iteration (with H = 255), the value in
L is decremented from 255 to 0 i.e., 255
times



15. Ans: (c)

Sol: Flags are not affected for execution of data transfer instructions since there is no involvement of ALU

16. Ans: (a)

Sol: Immediate addressing : LXI H, 2050H
Implied addressing : RRC
Register addressing : MOV A,B
Direct addressing : LDA 30FF

17. Ans: (c)

Sol: 'DAD' instruction adds contents of HL register pair with specified register pair contents and stored in HL register pair.

18. Ans: (a)

Sol: Format of instruction Template:-

Label	Mnemonics	operand	comments
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19. Ans: (b)

Sol: Implicit addressing mode
: RAL

Register-indirect addressing mode
: MOV A, M

Immediate addressing mode
: JMP 3FA0H

Direct addressing mode
: LDA 03FCH

20. Ans: (a)

Sol: Total no. of machine cycles in CALL instruction is 18.

1. Opcode fetch=6T

2. Two memory READ machine cycles to read subroutine address = 3T + 3T = 6T

3. Two memory WRITE machine cycles on the stack = 3T + 3T = 6T

∴ I/O was not used in CALL instruction

21. Ans: (d)

Sol: PCHL : Transfer the contents of HL to the program counter.

SPHL : Transfer the contents of HL to the stack pointer

XTHL : Exchange the top of the stack with the contents of HL pair

XCHG : Exchange the contains of HL with those of DE pair

01. Ans: (c)

Sol: 16-bit microprocessor has more speed and more data handling capability compared to 8-bit microprocessor.

02. Ans: (c)

Sol: In case of a 16-bit processor, a single instruction is enough to process a function. For processing the same function a long sequence of instructions will be required for a 8-bit processor.

03. Ans: (c)

Sol:

- 8086 μP has 20 Address output lines. As such, a total of about 2^{20} i.e., 1MB memory can be directly addressed by 8086 μP
- The programming model of 8086 μP has the following registers
AX, BX, CX, DX
CS, DS, SS, ES
Flag registers: SP, IP, BP, SI, DI i.e., a total no. of 14 registers
- There are total 9 flags in 8086 μP and the flag register is divided into two types.
 - (a) Status flags: The six status flags are
 1. Sign flag (S)
 2. Zero flag (Z)
 3. Auxiliary carry flag (AC)
 4. Parity flag (P)
 5. Carry flag (CY)
 6. Overflow flag (O)
 - (b) Control flags: The three control flags are
 1. Directional flag (D)
 2. Interrupt flag (I)
 3. Trap flag (T)

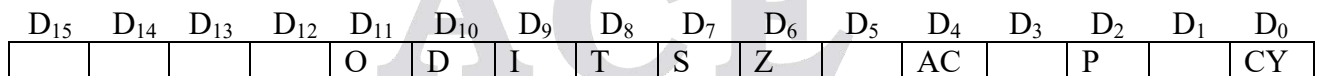


Fig: Format of flag register

04. Ans: (c)

Sol: Setting Trap flag puts the processor into single mode for debugging. In single stepping microprocessor executes an instruction and enters into single step ISR. If $TF = 1$, the CPU automatically generates an internal interrupt after each instruction, allowing a program to be inspected as it executes instruction by instruction.

05. Ans: (b)

Sol: For 8086 μP , the jump distance in bytes for short jump range is forward 127 and backward 128.

06. Ans: (a)

Sol: Number of address lines in 8086 is 20. Address space is $2^{20} = 1\text{MB}$



07. Ans: (d)

Sol: The instruction queue length in 8086 is 6 bytes and in 8088 is 4 bytes.

08. Ans: (d)

Sol: 8086 microprocessor can be operated in multiprocessor configuration when $\overline{MN}/\overline{MX}$ input connected to ground.

09. Ans: (d)

Sol: A 16 bit μP completes access of a word starting from even address in one bus cycle.

10. Ans: (b)

Sol: In relative base indexed Addressing mode, the 20 bit physical address of Data segment location is calculated as followed.

$$\begin{aligned} P.A &= (D.S \text{ register}) \times 10H + (B \times \text{register}) \\ &\quad + (DI \text{ register}) + 16 \text{ bit displacement} \\ &= 2100H \times 10H + 0158H + 1045H \\ &\quad + 1B57H \\ &= 21000H + 2CF4H \\ &= 23CF4H \end{aligned}$$

11. Ans: (a)

Sol: Effective Address = $(C.S \text{ reg}) \times 10H$
+ (IP reg)
= $1FABH \times 10H + 10A1H$
= 20B51H

12. Ans: (c)

Sol: SI is the source index, used as a pointer to the current character being read in a string instruction. It is also available as an offset to add to BX or BP when doing indirect addressing.

DI is the destination index, used as a pointer to the current character being written or compared in a string instruction. It is also available as an offset.

13. Ans: (b)

Sol: The intermediate wait states are always, inserted between the clock cycles T_2 and T_3 .

14. Ans: (a)

Sol: For a type 0 interrupt, the 8086 pushes the flag register on the stack, resets IF and TF and pushes the return addresses on the stack.

15. Ans: (c)

Sol: The interrupt vector table IVT of 8086 contains the starting CS and IP values of the interrupt service routine.

16. Ans: (d)

Sol: The 8086 arithmetic instructions work on Signed and unsigned numbers Unpacked BCD data

17. Ans: (c)

Sol: LOOP and ROTATE instructions of an 8086 μp uses the contents of a CX register as a counter.

18. Ans: (c)

Sol: In a multi-processor configuration, the two co-processor instruction sets must be disjoint.

19. Ans: (b)

Sol: MOV [1234 H], AX
Move the contents of register AX to memory offset 1234 H and 1235 H.

01. Ans: (c)

Sol: Out of the 128-byte internal RAM of the 8051, only 16 bytes are bit-addressable. The bit-addressable RAM locations are 20H to 2FH

02. Ans: (a)

Sol: The internal RAM size is 128 bytes and internal ROM size is 4KB.

03. Ans: (a)

Sol: In the 8051, the stack pointer points to the last used location of the stack. As we push data onto the stack, the stack pointer is incremented by one.

04. Ans: (c)

Sol:

$$\begin{array}{r} (A) = 9CH = 1001\ 1100 \\ +64H = 0110\ 0100 \\ \hline 0000\ 0000 \end{array}$$

AC = 1 since there is a carry from bit D3 to bit D4

CY = 1 since there is a carry from bit D7

P = 0 since there are zero 1s in result i.e., Even Parity.

05. Ans: (c)

Sol: ORG is a Assembler directive that directs the assembler to store the program code from 2000H.

This will not be converted into machine code.

06. Ans: (c)

Sol: RAM memory space allocation in the 8051

7F		Scratch pad RAM
30		
2F		Bit addressable RAM
20		
1F		Register Bank 3
18		
17		Register Bank 2
10		
0F		Register Bank 1
08		
07		Register Bank 0
00		

07. Ans: (d)

Sol: The given question is in incorrect format. The question is: On power UP, the 8051 uses RAM location _____ for register R0. The answer is 08H.

01. Ans: (b)

Sol: A real time embedded system is defined as, a system which gives a required output in a particular time. These types of embedded systems follow the time deadlines for completion of a task.

So, Microwave oven is a real time embedded system.

02. Ans: (b)

Sol: A system on chip (SOC) is an integrated circuit commonly applied in the area of embedded system.

03. Ans: (d)

Sol: When selecting a processor in an embedded system one should take instruction set, processor ability and max bits in the operand into consideration.

04. Ans: (a)

Sol: The Inter-integrated circuit (I2C) is a protocol intended to allow multiple slave digital integrated circuits (chips) to communicate with one or more master chips.

