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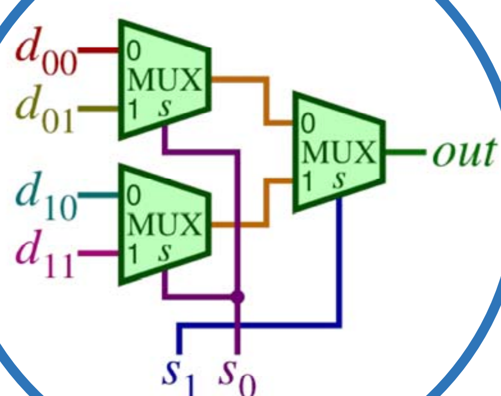

GATE | PSUs

DIGITAL CIRCUITS & MICROPROCESSORS

Volume - I : Study Material with Classroom Practice Questions

Study Material with Classroom Practice solutions

To

Digital Circuits & Microprocessors

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Chapter 1

Number Systems

Class Room Practice Solutions

01. Ans: (d)

Sol: $135_x + 144_x = 323_x$

$(1\times x^2 + 3 \times x^1 + 5 \times x^0)+(1\times x^2+4\times x^1+ 4\times x^0) = 3x^2 + 2x^1 + 3x^0$

$\Rightarrow x^2+3x+5+x^2+4x+4 = 3x^2+ 2x + 3$

$x^2 - 5x - 6 = 0$

$(x-6)(x+1) = 0$ (Base cannot be negative)

Hence x = 6.

(OR)

As per the given number x must be greater than 5. Let consider x = 6

$(135)_6 = (59)_{10}$

$(144)_6 = (64)_{10}$

$(323)_6 = (123)_{10}$

$(59)_{10} + (64)_{10} = (123)_{10}$

So that x = 6

02. Ans: (a)

Sol: 8-bit representation of $+127_{10}$

$= 01111111_{(2)}$

1's complement representation of

– 127 = 10000000.

2's complement representation of

– 127 = 10000001.

No. of 1's in 2's complement of

– 127 = m = 2

No. of 1's in 1's complement of

– 127 = n = 1

$\therefore$ m: n = 2:1

03. Ans: (c)

Sol: In 2's complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is 'X_3', hence it can be extended left any no. of times.

04. Ans: (c)

05. Ans: 5

Sol: Symbols used in this equation are 0,1,2,3 Hence base or radix can be 4 or higher

$(312)_x = (20)_x\ (13.1)_x$

$3x^2 + 1x + 2x^0 = (2x+0)(x+3x^0+x^{-1})$

$3x^2+x+2 = (2x)\left(x + 3 + \frac{1}{x}\right)$

$3x^2 + x + 2 = 2x^2 + 6x + 2$

$x^2 - 5x = 0$

$x(x-5) = 0$

x = 0(or) x = 5

x must be x > 3, So x = 5

06. Ans: 3 possible solutions

Sol: $123_5 = x8_y$

$1 \times 5^2 + 2 \times 5^1 + 3\times 5^0 = x.y^1 + 8 \times y^0$

$25 + 10 + 3 = xy+8$

$\therefore xy = 30$

Possible solutions:

i. x = 1, y = 30

ii. x = 2, y = 15

iii. x = 3, y = 10

3 possible solutions

07. Ans: (1)

Sol: The range (or) distinct values

For 2's complement $\Rightarrow -(2^{n-1})$ to $+(2^{n-1}-1)$

For sign magnitude

$\Rightarrow -(2^{n-1}-1)$ to $+(2^{n-1}-1)$

Let n = 2 $\Rightarrow$ in 2's complement

$-(2^{2-1})$ to $+(2^{2-1}-1)$

-2 to $+1 \Rightarrow -2, -1, 0, +1 \Rightarrow x = 4$

n = 2 in sign magnitude $\Rightarrow -1$ to $+1 \Rightarrow y = 3$

$x - y = 1$

Chapter 2 Logic Gates & Boolean Algebra

Class Room Practice Solutions

01. Ans: (c)

Sol: Given 2's complement numbers of sign bits are x & y. z is the sign bit obtained by adding above two numbers. ∴ Overflow is indicated by $= \bar{x}\,\bar{y}\,z + x\,y\,\bar{z}$

Examples

1. A = +7 0111
   B = +7 0111
   14 1110 ⇒ $\bar{x}\,\bar{y}\,z$
2. A = +7 0111
   B = +5 0101
   12 1100 ⇒ $\bar{x}\,\bar{y}\,z$
3. A = –7 1001
   B = –7 1001
   –14 10010 ⇒ $x\,y\,\bar{z}$
4. A = –7 0111
   B = –5 0101
   –12 10100 ⇒ $x\,y\,\bar{z}$

02. Ans: (b)

Sol: Truth table of XOR

A	B	o/p
0	0	0
0	1	1
1	0	1
1	1	0

Stage 1:

Given one i/p = 1 Always.

1	X	o/p	
1	0	1	$= \bar{X}$
1	1	0	$= \bar{X}$

For First XOR gate o/p = $\bar{X}$

Stage 2:

$\bar{X}$	X	o/p
0	1	1
1	0	1

For second XOR gate o/p = 1.

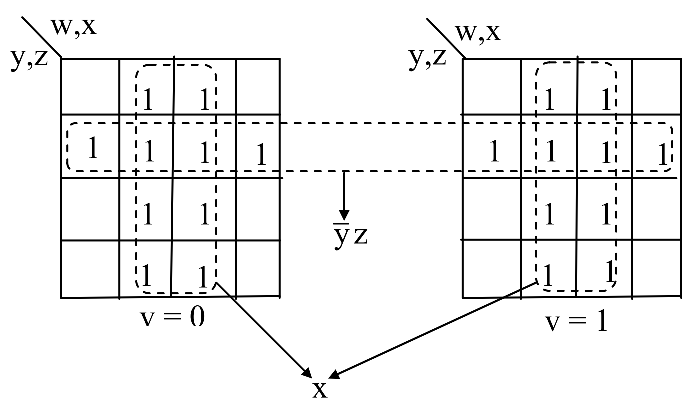
Similarly for third XOR gate o/p = $\bar{X}$ & for fourth o/p = 1

For Even number of XOR gates o/p = 1

For 20 XOR gates cascaded o/p = 1.

03. Ans: (b)

Sol:

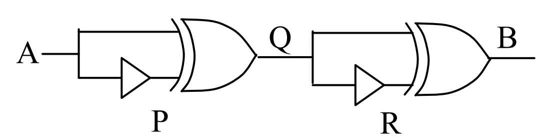


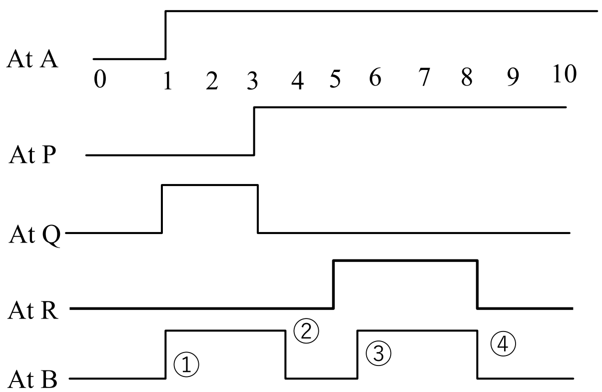
04. Ans: (c)

Sol: $f = f_1 f_2 + f_3$

05. Ans: (d)

Sol:





06. Ans: (c)

Sol: For all cases option A, B, D not satisfy.

07. Ans: (b)

Sol: $M(a,b,c) = ab + bc + ca$

$\overline{M(a,b,c)} = \bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c}$

$M(a, b, \bar{c}) = ab + b\bar{c} + \bar{c}a$

$M(\overline{M(a,b,c)}, M(a,b,\bar{c}), c)$

$= (\bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c})(ab + b\bar{c} + a\bar{c}) + (ab + b\bar{c} + \bar{c}a)c + (\bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c})c$

$= (\bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c})(ab + b\bar{c} + a\bar{c}) + (\bar{b}\bar{c} + \bar{a}\bar{b} + \bar{a}\bar{c})(c) + abc$

$= a\bar{b}\bar{c} + \bar{a}b\bar{c} + abc + \bar{a}\bar{b}c$

$= \bar{c}[a\bar{b} + \bar{a}b] + c[ab + \bar{a}\bar{b}]$

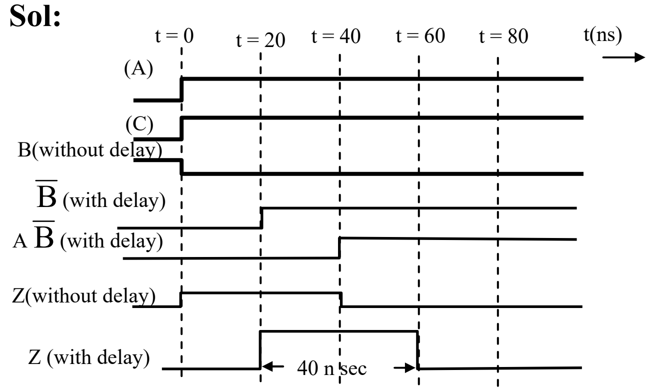
$= \sum m(1, 2, 4, 7)$

$\therefore M(x, y, z) = a \oplus b \oplus c$

Where $x = \overline{M(a,b,c)}$, $y = M(a,b,\bar{c})$, $z = c$

08. Ans: 40

Sol:



$\therefore$ Z is 1 for 40 nsec

09. Ans: (c)

Sol: Logic gates $\bar{X} + Y = \overline{X\bar{Y}} = \overline{XY_1}$

Where $Y_1 = \bar{Y}$

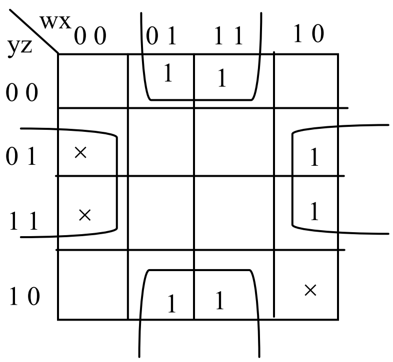
It is a NAND gate and thus the gate is 'Universal gate'.

Chapter 3 K - Maps

Class Room Practice Solutions

01. Ans: (b)

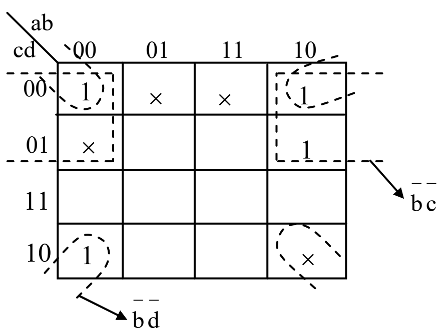
Sol:



$f = \bar{x}z + x\bar{z}$

02. Ans: (b)

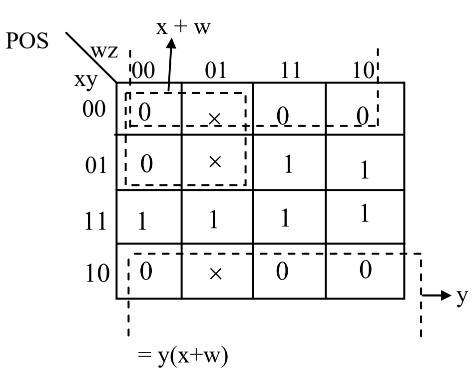
Sol:

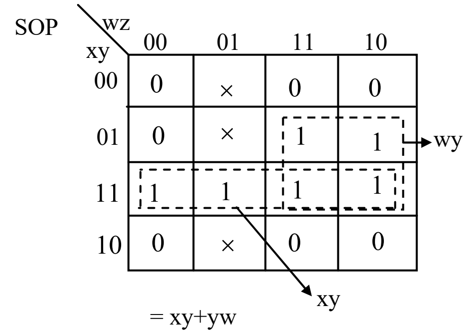


$f = \bar{b}\,\bar{d} + \bar{b}\,\bar{c}$

03.

Sol:





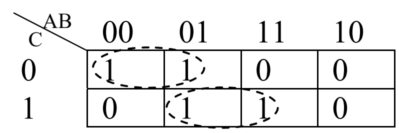
SOP: x y + y w

POS: y(x + w)

04. Ans: (a)

05. Ans: (c)

Sol:



$F(A, B, C) = \bar{A}\,\bar{C} + BC$

06. Ans: 1

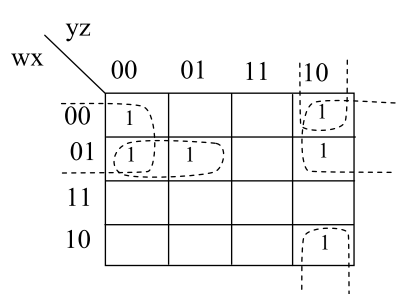
Sol: After minimization = $\left(\overline{\bar{A} + \bar{B} + \bar{C} + \bar{D}}\right)$

= ABCD

$\therefore$ only one minterm.

07. Ans: 3

Sol: $\overline{w}\,\overline{z} + \overline{w}\,x\overline{y} + \overline{x}\,y\overline{z}$



Chapter 4 Combinational Circuits

Class Room Practice Solutions

01. Ans: (d)

Sol: Let the output of first MUX is "F_1"

$F_1 = AI_0 + AI_1$

Where A is selection line, I_0, I_1 = MUX Inputs

$F_1 = \overline{S}_1.W + S_1.\overline{W} = S_1 \oplus W$

Output of second MUX is

$F = \overline{A}.I_0 + A.I_1$

$F = \overline{S}_2.F_1 + S_2.\overline{F}_1$

$F = S_2 \oplus F_1$

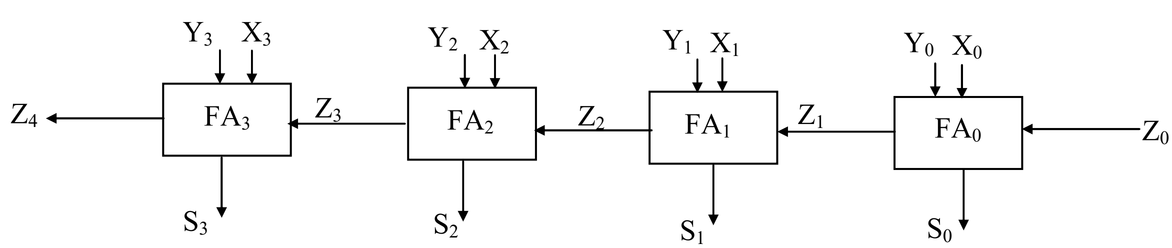
But $F_1 = S_1 \oplus W$

$F = S_2 \oplus S_1 \oplus W$

i.e., $F = W \oplus S_1 \oplus S_2$

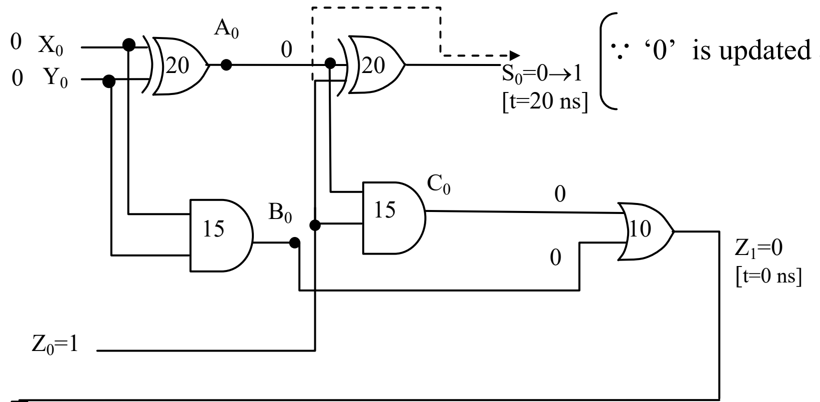
02. Ans: 50

Sol:



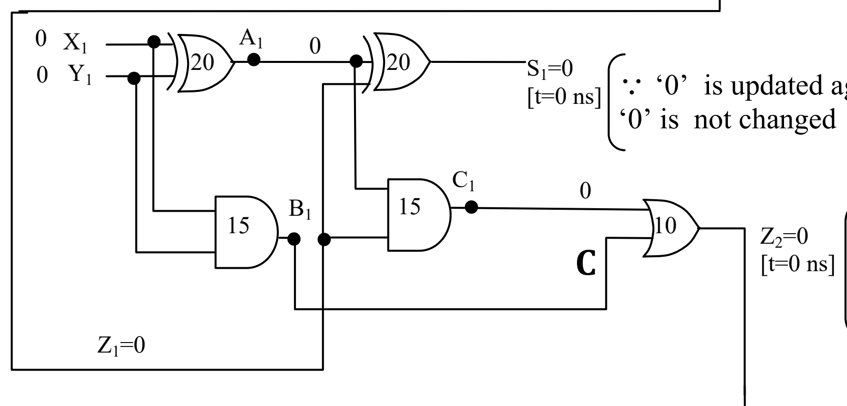
Initially all the output values are '0', at t = 0, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0 = 1100$, $Y_3Y_2Y_1Y_0 = 0100$

- - - - - - indicates critical path delay to get the output



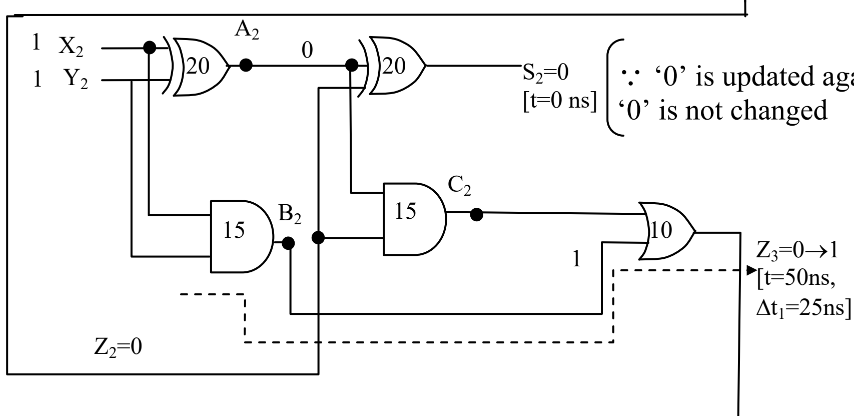
(∵ '0' is updated as '1' after 20ns)

(∵ '0' is updated again to '0' (or) '0' is not changed, i.e. Z_1 is available @ t= 0 ns)



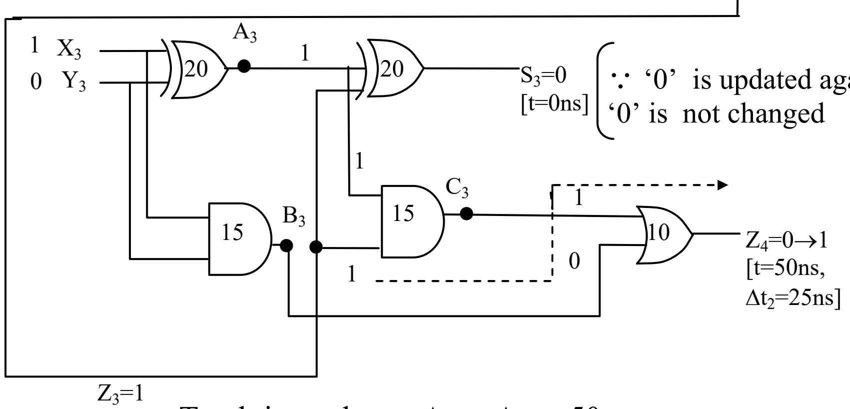
(∵ '0' is updated again to '0' (or) '0' is not changed)

(∵ '0' is updated again to '0' (or) '0' is not changed, i.e. Z_2 is available @ t= 0 ns)



(∵ '0' is updated again to '0' (or) '0' is not changed)

(∵ '0' is updated to '1' after 25 ns)



(∵ '0' is updated again to '0' (or) '0' is not changed)

(∵ '0' is updated as '1' after 25ns when Z_3 is arrived)

Total time taken = $\Delta t_1 + \Delta t_2$ = 50 ns

i.e. critical time (or) maximum time is taken for Z_4 to get final output as '1'

03. Ans: (a)

Sol: The given circuit is binary parallel adder/subtractor circuit. It performs A+B, A–B but not A + 1 operations.

K	C_0	Operation
0	0	A+B (addition)
0	1	A+B+1(addition with carry)
1	0	$A+\overline{B}$ (1's complement addition)
1	1	$A+\overline{B}+1$(2's complement subtraction)

04. Ans: (d)

Sol: It is expansion of 2:4 decoders to 1:8 demultiplexer A_1, A_0 must be connected to S_1, S_0 i.e.., $R = S_0$, $S = S_1$

Q must be connected to S_2 i.e., $Q = S_2$

P is serial input must be connected to D_{in}

05. Ans: 6

Sol: T = 0 → NOR → MUX 1 → MUX 2

2ns 1.5ns 1.5ns

Delay = 2ns + 1.5ns + 1.5ns = 5ns

T = 1 → NOT → MUX 1→NOR→ MUX 2

1ns 1.5ns 2ns 1.5ns

Delay = 1ns + 1.5ns + 2ns + 1.5ns = 6ns

Hence, the maximum delay of the circuit is 6ns

06. Ans: –1

Sol: When all bits in 'B' register is '1', then only it gives highest delay.

∴ '–1' in 8 bit notation of 2's complement is 1111 1111

Chapter **5**

Sequential Circuits

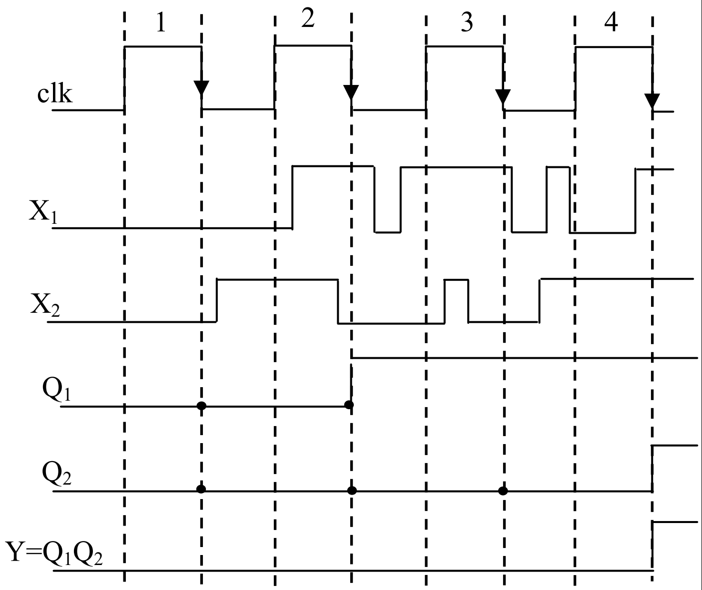
Class Room Practice Solutions

01. Ans: (c)

Sol: Given Clk, X_1, X_2

Output of First D–FF is Q_1

Output of Second D–FF is Q_2



02. Ans: 4

Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

03. Ans: 7

Sol: The counter is cleared when

$Q_DQ_CQ_BQ_A = 0110$

Clk	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	0	0

As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get's cleared during the 7th clock pulse.

$\therefore$ mod of counter = 7

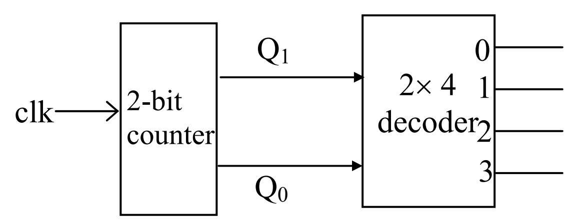
04. Ans: (b)

Sol: The given circuit is a mod 4 ripple down counter. Q_1 is coming to 1 after the delay of $2\Delta t$.

CLK	Q_1	Q_0
	0	0
1	1	1
2	1	0
3	0	1
4	0	0

05. Ans: (c)

Sol: Assume n = 2



Outputs of counter is connected to inputs of decoder

Counter outputs		Decoder inputs		Decoder outputs			
Q_1	Q_0	a	b	d_3	d_2	d_1	d_0
0	0	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0

The overall circuit acts as 4-bit ring counter

n = 2

$\therefore k = 2^2 = 4$, k-bit ring counter

06. Ans: (b)

Sol:

CLK	Serial in= $B\oplus C\oplus D$	A B C D
0		1 0 1 0
1	1 →	1 1 0 1
2	0 →	0 1 1 0
3	0 →	0 0 1 1
4	0 →	0 0 0 1
5	1 →	1 0 0 0
6	0 →	0 1 0 0
7	1 →	1 0 1 0

07. Ans: (b)

Sol:

J	K	Q	$\overline{Q}_n$	$T=(J+Q_n)(K+\overline{Q}_n)$	Q_{n+1}
0	0	0	1	0.1 = 0	0 } Q_n
0	0	1	0	1.0 = 0	1
0	1	0	1	0.1 = 0	0 } 0
0	1	1	0	1.1 = 1	0
1	0	0	1	1.1 = 1	1 } 1
1	0	1	0	1.0 = 0	1
1	1	0	1	1.1 = 1	1 } $\overline{Q}_n$
1	1	1	0	1.1 = 1	0

J \ KQ_n	00	01	11	10
0			1	
1	1		1	1

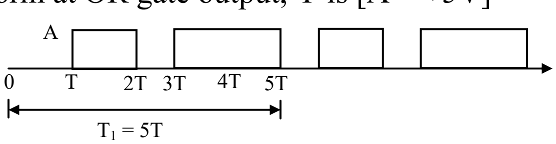
$$T = J\overline{Q_n} + KQ_n = (J+Q_n)(K+\overline{Q_n})$$

08. Ans: 1.5

Sol:

Clk	Q_1	Q_2	Q_3	Q_4	Q_5	$Y = Q_3 + Q_5$
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0

The waveform at OR gate output, Y is [A = +5V]



Average power

$$P=\frac{V_{Ao}^2}{R}=\frac{1}{R}\left[\underset{T_1\to\infty}{Lt}\frac{1}{T_1}\int_o^{T_1}y^2(t)\,dt\right]=\frac{1}{RT_1}\left[\int_T^{2T}A^2dt+\int_{3T}^{5T}A^2dt\right]$$

$$=\frac{A^2}{RT_1}\left[(2T-T)+(5T-3T)\right]=\frac{A^2.3T}{R(5T)}=\frac{5^2.3}{10\times 5}=1.5\,mw$$

09. Ans: (b)

Sol:

Present State	Next State		Output (Y)	
	X = 0	X = 1	X = 0	X = 1
A	A	E	0	0
B	C	A	1	0
C	B	A	1	0
D	A	B	0	1
E	A	C	0	1

Step (1):

By replacing state B as state C then state B, C are equal.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
B	B	A
D	A	B
E	A	B

Step (2):

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
D	A	B
E	A	B

State D, E are equal, remove state E and replace E with D in next state.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B
D	A	B

Finally reduced state table is

Reduced state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B

∴ 3 states are present in the reduced state table

10. Ans: (c)

Sol: State table for the given state diagram

State	Input	Output
S_0	0	1
S_0	1	0
S_1	0	1
S_1	1	0

Output is 1's complement of input.

11. Ans: (c)

Sol: In state (C), when XYZ = 111, then Ambiguity occurs

Because, from state (C)

⇒ When X = 1, Z = 1

⇒ N.S is (A)

When Y = 1, Z = 1 ⇒ N.S is (B)

Chapter 6 Logic Gate Families

Class Room Practice Solutions

01. Ans: (b)

Sol: V_{OH}(min):-

(High level output voltage)

The minimum voltage level at a Logic circuit output in the logic '1' state under defined load conditions.

V_{OL}(max):-

(Low level output voltage)

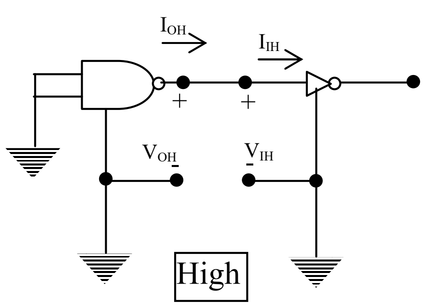
The maximum voltage level at a logic circuit output in the Logical '0' state under defined load conditions.

V_{IL}(max):- (Low level input voltage)

The maximum voltage level required for a logic '0' at an input. Any voltage above this level will not be accepted as a Low by the logic circuit.

V_{IH}(min) :- (High level Input voltage)

The minimum voltage level required for logic '1' at an input. Any voltage below this level will not be accepted as a HIGH by the Logic circuit.



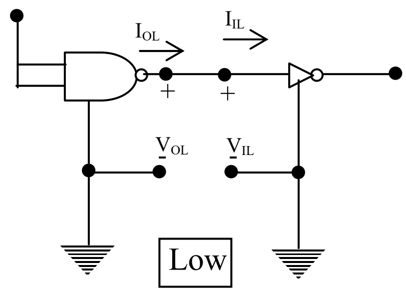


Fig: currents and voltages in the two logic states.

02. Ans: (b)

Sol: Fan out is minimum in DTL

(High Fan-out = CMOS)

Power consumption is minimum in CMOS. Propagation delay is minimum in ECL (fastest = ECL)

03. Ans: (b)

04. Ans: (d)

05. Ans: (b)

Sol: As per the description of the question, when the transistor Q_1 and diode both are OFF then only output z = 1.

X	Y	Z	Remarks
0	0	0	Q_1 is OFF, Diode is ON
0	1	1	Q_1 is OFF, Diode is OFF
1	0	0	Q_1 is ON, Diode is OFF
1	1	0	Q_1 is ON, Diode is OFF

Hence $Z = \overline{X}Y$

Chapter **7**

Semiconductor Memories

Class Room Practice Solutions

01. Ans: (b)

Sol: Square of a 4 – bit number can be at most 8 – bit number.

{ i.e $(1111)_2 = (15)_{10}$

$[(15)_{10}]^2 = (225)_{10}$}.

Therefore ROM requires 8 data lines.

Data is with size of 4 bits

ROM must require 4 address lines and 8 data lines

ROM = $2^n \times m$

n = inputs(address lines),

m = output lines

n = 4, m = 8.

02. Ans: (a)

Sol: ROM is used to design a combinational circuit. The number of address lines of the ROM is equal to the number of input variables in the truth table.

ROM is represented as $2^n \times m$ where 2^n inputs and m output lines.

[Where n = address bits]

03. Ans: (b)

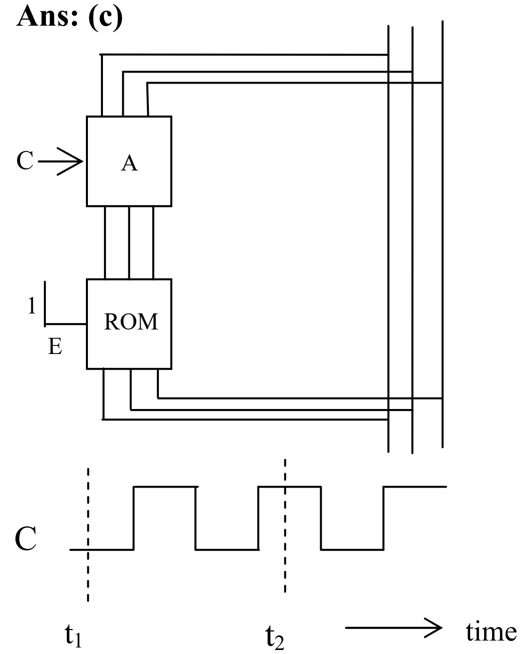
Sol:

8	4	2	1	2	4	2	1	2421 Outputs
i/p s				o/p s				
X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0	
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	3
0	1	0	0	0	1	0	0	4
0	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	6
0	1	1	1	1	1	0	1	7
1	0	0	0	1	1	1	0	8
1	0	0	1	1	1	1	1	9
1	0	1	0	×	×	×	×	
1	0	1	1	×	×	×	×	
1	1	0	0	×	×	×	×	
1	1	0	1	×	×	×	×	
1	1	1	0	×	×	×	×	
1	1	1	1	×	×	×	×	

The outputs are in 2 4 2 1 BCD number

04. Ans: (c)

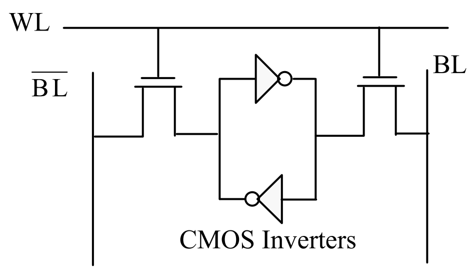
Sol:



At the rising edge of the First clock pulse the content of location $(0110)_2$ = 6 ⇒ 1010 appears on the data bus, at the rising of the second clock pulse the content of location $(1010)_2 = 10_2 \Rightarrow 1000$ appears on the data bus.

05. Ans: (b)

Sol: 1–bit SRAM memory cell is



In 2 Inverters, output of the 1st Inverter is connected to Gate Input of 2nd Inverter and vice versa.

Chapter **8**

A/D & D/A Converters

Class Room Practice Solutions

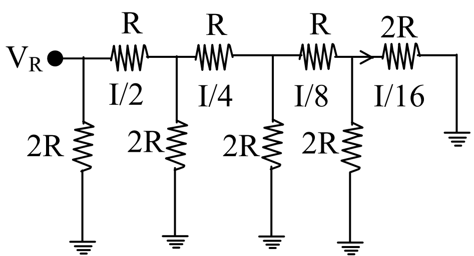
01. Ans: (b)

Sol:

CLK	Counter			Decoder				V_0
	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1	1
3	0	1	0	0	0	1	0	2
4	0	1	1	0	0	1	1	3
5	1	0	0	1	0	0	0	8
6	1	0	1	1	0	0	1	9
7	1	1	0	1	0	1	0	10
8	1	1	1	1	0	1	1	11

02. Ans: (b)

Sol:



R_{equ} = (((((2R||2R)+R)||2R)+R)||2R)+R)||2R)

$R_{equ} = R = 10k\Omega$.

$$I = \frac{V_R}{R} = \frac{10V}{10k} = 1mA.$$

Current division at $\frac{I}{16}$

$$= \frac{1\times10^{-3}}{16} = 62.5\,\mu A$$

03. Ans: (c)

Sol: Net current at inverting terminal,

$$I_i = \frac{I}{4} + \frac{I}{16} = \frac{5I}{16}$$

$$V_0 = -I_i R = -\frac{5I}{16}\times 10k\Omega$$

$$= \frac{-5\times1\times10^{-3}\times10\times10^{3}}{16} = -3.125V$$

04. Ans: (d)

Sol: Given that $V_{DAC} = \sum_{n=0}^{3} 2^{n-1} b_n$ Volts

$$V_{DAC} = 2^{-1}b_0 + 2^0 b_1 + 2^1 b_2 + 2^2 b_3$$

$\Rightarrow V_{DAC} = 0.5b_0 + b_1 + 2b_2 + 4b_3$

Initially counter is in 0000 state

Up counter o/p $b_3\ b_2\ b_1\ b_0$	V_{DAC}(V)	o/p of comparator
0 0 0 0	0	1
0 0 0 1	0.5	1
0 0 1 0	1	1
0 0 1 1	1.5	1
0 1 0 0	2	1
0 1 0 1	2.5	1
0 1 1 0	3	1
0 1 1 1	3.5	1
1 0 0 0	4	1
1 0 0 1	4.5	1
1 0 1 0	5	1
1 0 1 1	5.5	1
1 1 0 0	6	1
1 1 0 1	6.5	0

When V_{DAC} = 6.5 V, the o/p of comparator is '0'. At this instant, the clock pulses to the counter are stopped and the counter remains in 1101 state.

$\therefore$ The stable reading of the LED display is 13.

05. Ans: (b)

Sol: The magnitude of error between V_{DAC} & V_{in} at steady state is $|V_{DAC} - V_{in}| = |6.5 - 6.2|$

$= 0.3$ V

06. Ans: (a)

Sol: In Dual slope

ADC $\Rightarrow V_{in}T_1 = V_R.T_2$

$$\Rightarrow V_{in} = \frac{V_R T_2}{T_1}$$

$$= \frac{100\,\text{mV} \times 370.2\,\text{ms}}{300\text{ ms}}$$

$\text{DVM indicates} = 123.4$

07. Ans: (d)

Sol: Ex: $f_{in} = 1$ kHz $\rightarrow f_s = 2$ kHz

$f_{in} = 25$ kHz $\leftarrow f_s = 50$ kHz

1. Max conversion time = $2^{N+1}T = 2^{11}.1\ \mu s$

   $= 2048\ \mu s$

2. Sampling period = $T_s \geq$ maximum conversion time

   $T_s \geq 2048\ \mu s$

3. Sampling rate $f_s = \dfrac{1}{T_s} \leq \dfrac{1}{2048 \times 10^{-6}}$

   $f_s \leq 488 \quad f_s \leq 500$ Hz

4. $f_{in} = \dfrac{f_s}{2} = 250\,\text{Hz}$

Chapter **9**

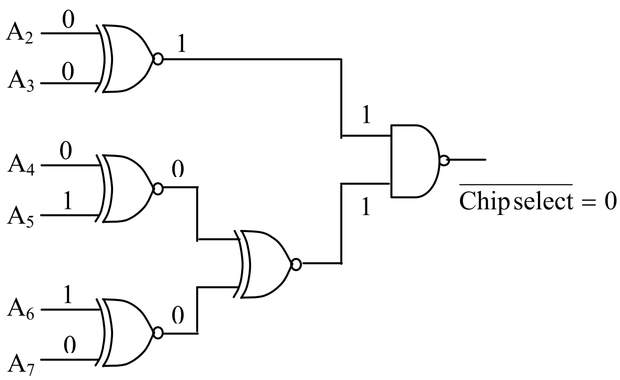
Architecture, Pin Details of 8085 & Interfacing with 8085

Class Room Practice Solutions

01. Ans: (a)

Sol: A_0 & A_1 are used for line selection

A_2 to A_7 are used for chip selection



∴ Address space is 60H to 63H

A_o to A_{11} are used for line selection

A_{12} to A_{15} are used for chip selection

A_{15}	A_{14}	A_{13}	A_{12}	A_{11} - - - - - A_0	
1	1	1	0	0 - - - - - - - 0	=E000H
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	0	1 - - - - - - - - 1	=EFFFH

02. Ans: (d)

Sol:

- Both the chips have active high chip select inputs.
- Chip 1 is selected when $A_8 = 1$, $A_9 = 0$
  Chip 2 is selected when $A_8 = 0$, $A_9 = 1$
- Chips are not selected for combination of 00 & 11 of A_8 & A_9
- Upon observing A_8 & A_9 of given address Ranges, F800 to F9FF is not represented

03. Ans: (d)

Sol: The I/O device is interfaced using "Memory Mapped I/O" technique.

The address of the Input device is

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	$=F8F8_H$

The Instruction for correct data transfer is = LDA F8F8H

04. Ans: (b)

Sol:

- Out put 2 of 3×8 Decoder is used for selecting the output port. ∴ Select code is 010

  A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} -- A_0

  0 1 0 1 0 0 --- - 0

  ⇒ 5000H
- This mapping is memory mapped I/o

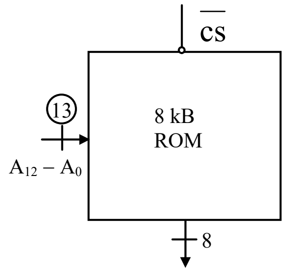
05. Ans: (d)

Sol:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9 - - - - A_0	
0	0	0	0	1	0	0 - - - - 0	=0800H
		⋮				⋮	⋮
0	0	0	0	1	0	1 - - - - 1	=0BFFH
0	0	0	1	1	0	0 - - - - 0	=1800H
		⋮				⋮	⋮
0	0	0	1	1	0	1 - - - - 1	=1BFFH
0	0	1	0	1	0	0 - - - - 0	=2800H
		⋮				⋮	⋮
0	0	1	0	1	0	1 - - - - 1	=2BFFH
0	0	1	1	1	0	0 - - - - 0	=3800H
		⋮				⋮	⋮
0	0	1	1	1	0	1 - - - - 1	=3BFFH

06. Ans: (a)

Sol: Address Range given is



	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1000H →	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2FFFH →	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1

To provide $\overline{cs}$ as low, The condition is

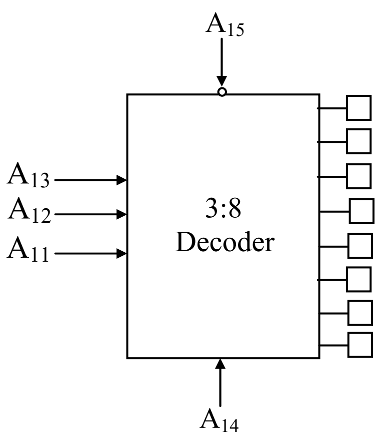
$A_{15} = A_{14} = 0$ and $A_{13}\ A_{12} = 01$ (or) (10)

i.e $A_{15} = A_{14} = 0$ and $A_{13}\ A_{12}$ shouldn't be 00, 11.

Thus it is $A_{15} + A_{14} + [A_{13}A_{12} + \overline{A_{13}}, \overline{A_{12}}\ ]$

07. Ans: (a)

Sol:



A_{15}, A_{14} are used for chip selection

A_{13}, A_{12}, A_{11} are used for input of decoder

A_{15} A_{14}	A_{13} A_{12} A_{11}	A_{10} ------ A_0
Enable of decoder	Input of decoder	Address of chip

Size of each memory block = 2^{11} = 2K

Chapter 10 Instruction set of 8085 & Programming with 8085

Class Room Practice Solutions

01. Ans: (c)

Sol:

6010H : LXI H,8A79H ; (HL) = 8A79H

6013H : MOV A, L ; (A)←(L) = 79

6014H : ADD H ; (A) = 0111 1001

+

; (H) = 1000 1010

; (A) = 0000 0011

CY = 1, AC = 1

6015H : DAA ; 66 Added to (A) since CY=1 & AC =1

; (A) = 69H

6016H : MOV H,A ; (H)←(A) =69H

6017H : PCHL ; (PC)←(HL) = 6979H

02. Ans: (c)

Sol: 0100H : LXI SP, 00FFH ; (SP) = 00FFH

0103H : LXI H, 0107 H ; (HL) = 0107H

0106H : MVI A, 20H ; (A) = 20H

0108H : SUB M ; (A)←(A)-(0107)

; (0107) = 20H

; (A) = 00H

The contents of Accumulator is 00H

03. Ans: (c)

Sol: SUB1 : MVI A, 00H A← 00H

CALL SUB2 → program will shifted to SUB 2 address location

SUB 2 : INR A → A: 01H

RET → returned to the main program

∴ The contents of Accumulator after execution of the above SUB2 is 02H

04. Ans: (c)

Sol: The loop will be executed until the value in register equals to zero, then,

Execution time

=9(7T+4T+4T+10T)+(7T+4T+4T+7T)+7T

= 254T

05. Ans: (d)

Sol: H=255 : L = 255, 254, 253, ----0

H=254 : L = 0, 255, 254, -------0

|

H=1 : L = 0,255,254,253,---0

H=0 : ——

→ In first iteration (with H=255), the value in L is decremented from 255 to 0 i.e., 255 times

→ In further remaining 254 iterations, the value in L is decremented from 0 to 0 i.e., 256 times

∴ 'DCRL' instruction gets executed for

$\Rightarrow [255 + (254 \times 256)]$

$\Rightarrow$ 65279 times

06. Ans: (a)

Sol: "STA 1234H" is a 3-Byte Instruction and it requires 4 Machine cycles (Opcode fetch, Operand1 Read, Operand2 Read, Memory write). The Higher order Address ($A_{15} - A_8$) sent in 4 machine cycles is as follows

Given "STA 1234" is stored at 1FFEH

i.e., Address Instruction

1FFE, 1FFF, 2000 : STA 1234H

Machine cycle	**Address (A_{15}-A_0)**	**Higher order address (A_{15}-A_8)**
1. Opcode fetch	1FFEH	1FH
2. Operand1 Read	1FFFH	1FH
3. Operand2 Read	2000H	20H
4. Memory Write	1234H	12H

i.e. Higher order Address sent on A_{15}-A_8 for 4 Machine Cycles are 1FH, 1FH, 20H, 12H.

07. Ans: (d)

Sol: The operation SBI BE_H indicates A-BE $\rightarrow$ A where A indicates accumulator

Thus the result of the subtraction operation is stored in the accumulator and the contents of accumulator are changed.

08. Ans: (c)

Sol: If the content in register B is to be multiplied with the content in register C, the contents of register B is added to the accumulator (initial value of accumulator is 0) for C times.