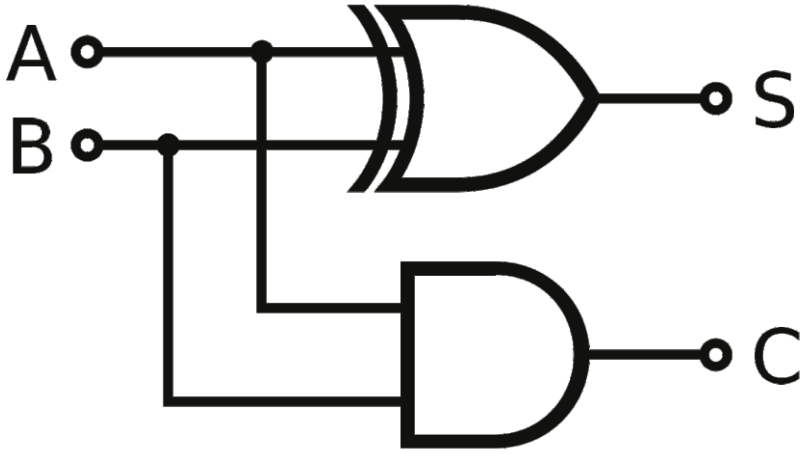
GATE | PSUs

COMPUTER SCIENCE & INFORMATION TECHNOLOGY

DIGITAL LOGIC

Volume - I : Study Material with Classroom Practice Questions



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Digital Logic

(Classroom Practice Booklet Solutions)

1. Number Systems

01. Ans: (d)

Sol: $(135)_x + (144)_x = (323)_x$

$(1\times x^2 + 3 \times x^1 + 5 \times x^0) + (1\times x^2 + 4\times x^1 + 4\times x^0)$

$= 3x^2 + 2x^1 + 3x^0$

$x^2+3x+5+x^2+4x+4 = 3x^2 + 2x + 3$

$x^2 - 5x - 6 = 0$

$(x-6)(x+1) = 0$ (Base cannot be negative)

Hence $x = 6$.

(OR)

As per the given number x must be greater than 5. Let consider x = 6

$(135)_6 = (59)_{10}$

$(144)_6 = (64)_{10}$

$(323)_6 = (123)_{10}$

$(59)_{10} + (64)_{10} = (123)_{10}$

So that x = 6

02. Ans: (a)

Sol: 8-bit representation of $+(127)_{10}$

$= (01111111)_{(2)}$

1's complement representation of

$-127 = 10000000.$

2's complement representation of

$-127 = 10000001.$

Number of 1's in 2's complement of

$-127 = m = 2$

Number of 1's in 1's complement of

$-127 = n = 1$

$\therefore$ m: n = 2:1

03. Ans: (c)

Sol: In 2's complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is 'X_3', hence it can be extended left any no. of times.

04. Ans: (c)

05. Ans: 5

Sol: Symbols used in this equation are 0,1,2,3

Hence base or radix can be 4 or higher

$(312)_x = (20)_x\ (13.1)_x$

$3x^2 + 1x + 2x^0 = (2x + 0)(x + 3x^0 + x^{-1})$

$$3x^2 + x + 2 = (2x)\left(x + 3 + \frac{1}{x}\right)$$

$3x^2 + x + 2 = 2x^2 + 6x + 2$

$x^2 - 5x = 0$

$x(x-5) = 0$

$x = 0$ (or) $x = 5$

x must be $x > 3$, So $x = 5$

06. Ans: 3

Sol: $(123)_5 = (x8)_y$

$1 \times 5^2 + 2 \times 5^1 + 3 \times 5^0 = x.y^1 + 8 \times y^0$

$25 + 10 + 3 = xy + 8$

$\therefore \quad xy = 30$

Possible solutions:

i. $x = 1, y = 30$

ii. $x = 2, y = 15$

iii. $x = 3, y = 10$

3 possible solutions

07. Ans: 1

Sol: The range (or) distinct values

For 2's complement $\Rightarrow -(2^{n-1})$ to $+(2^{n-1}-1)$

For sign magnitude

$\Rightarrow -(2^{n-1}-1)$ to $+(2^{n-1}-1)$

Let $n = 2 \Rightarrow$ in 2's complement

$-(2^{2-1})$ to $+(2^{2-1}-1)$

-2 to $+1 \Rightarrow -2, -1, 0, +1 \Rightarrow X = 4$

$n = 2$ in sign magnitude $\Rightarrow -1$ to $+1$

$\Rightarrow Y = 3$

$X - Y = 1$

08. Ans: 3

Sol:

0 1 1 0	0 0 1 0	0 1 0 0
0 1 0 0	1 0 0 1	0 1 1 0
1 0 1 0	1 0 1 1	1 0 1 0
0 1 1 0	0 1 1 0	0 1 1 0
0 0 0 0	0 0 0 1	0 0 0 0
1 ←	+ ← C=1	+ ← C=1
0001	0001	0010

09. Ans: +7

Sol: $(211)_x = (152)_8$

$2x^2 + x = 105$

$x = +7$ (or) -7.5

Answer is +7

10. Ans: (c)

Sol: Given 2's complement numbers of sign bits are x & y. z is the sign bit obtained by adding above two numbers.

$\therefore$ Overflow is indicated by $= \bar{x}\,\bar{y}\,z + x\,y\,\bar{z}$

Examples

1. A = +7 0111
   B = +7 0111
   14 1110 $\Rightarrow \bar{x}\,\bar{y}\,z$

2. A = +7 0111
   B = +5 0101
   12 1100 $\Rightarrow \bar{x}\,\bar{y}\,z$

3. A = –7 1001
   B = –7 1001
   –14 10010 $\Rightarrow x\,y\,\bar{z}$

4. A = –7 0111
   B = –5 0101
   –12 10100 $\Rightarrow x\,y\,\bar{z}$

2. Logic Gates and Boolean Algebra

01. Ans: 5

02. Ans: (b)

Sol: Truth table of XOR

A	B	O/P
0	0	0
0	1	1
1	0	1
1	1	0

Stage 1:

Given one I/P = 1 Always.

1 X O/P

---

1 0 1 = $\overline{X}$

1 1 0 = $\overline{X}$

For First XOR GATE

O/P = $\overline{X}$

Stage 2:

$\overline{X}$ X O/P

---

0 1 1

1 0 1

For second XOR GATE O/P=1.

Similarly for third XOR GATE O/P = $\overline{X}$ &

For fourth O/P=1

For Even number of XOR GATES O/P =1

For 20 XOR GATES CACADED O/P = 1.

03.

Sol: Given

0 1 0 1 1 0 1 0 → SBC = 1 0 1 0 0 1 0 1

→ CTC = 0 1 0 1 1 0 0 1

04. Ans: (c)

Sol: $f = f_1 f_2 + f_3$

05. Ans: (d)

Sol: Follow the path from First EX-OR to last EX-OR.

06. Ans: (c)

Sol: For all cases option a, b, d not satisfy.

07. Ans: (c)

Sol: Logic gates $\overline{X} + Y = \overline{X\overline{Y}} = \overline{XY_1}$

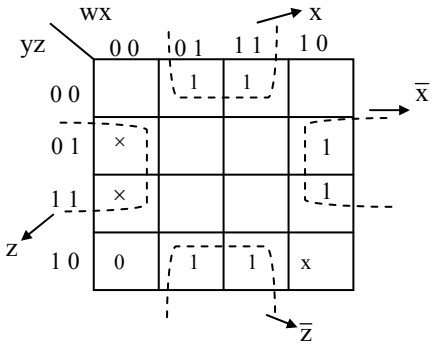
Where $Y_1 = \overline{Y}$

It is a NAND gate and thus the gate is 'Universal gate'.

3. K - Maps

01. Ans: (b)

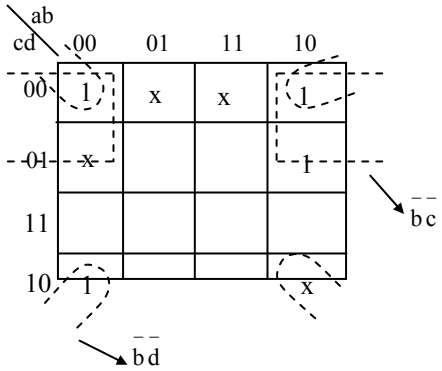
Sol:



$x\bar{z}+z\bar{x}$

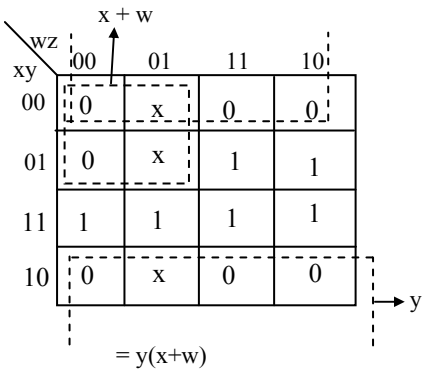
02. Ans: (b)

Sol:



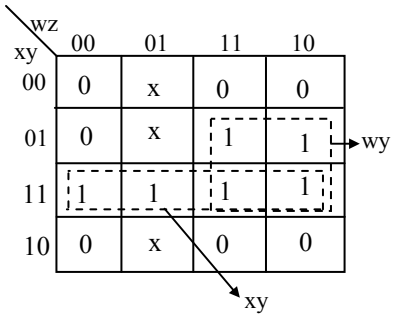
03.

Sol: **POS**



= y(x+w)

SOP



= xy+yw

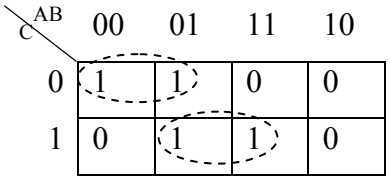
SOP: x y + y w

POS: y(x + w)

04. Ans: (a)

05. Ans: (c)

Sol:



$F(A,B,C) = \bar{A}\bar{C}+BC$

06. Ans: 1

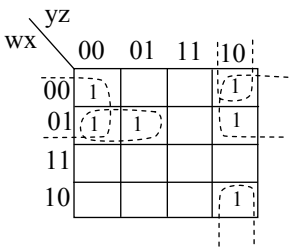
Sol: After minimization = $\left(\overline{\bar{A}+\bar{B}+\bar{C}+\bar{D}}\right)$

= ABCD

$\therefore$ only one minterm.

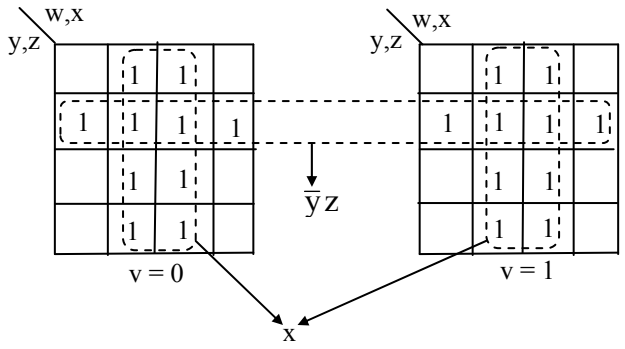
07. Ans: 3

Sol: $\bar{w}\bar{z}+\bar{w}x\bar{y}+\bar{x}\,yz$



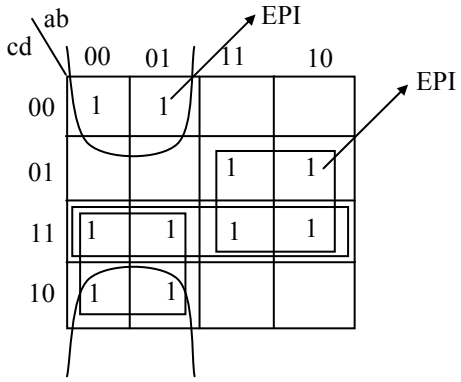
08. Ans: (b)

Sol:



09. Ans: 2

Sol:



4. Combinational Circuits

01. Ans: (d)

Sol: Let the output of first MUX is "F_1"

$F_1 = AI_0 + AI_1$

Where A is selection line, I_0, I_1 = MUX Inputs

$F_1 = \overline{S}_1.W + S_1.\overline{W} = S_1 \oplus W$

Output of second MUX is

$F = \overline{A}.I_0 + A.I_1$

$F = \overline{S}_2.F_1 + S_2.\overline{F}_1$

$F = S_2 \oplus F_1$

But $F_1 = S_1 \oplus W$

$F = S_2 \oplus S_1 \oplus W$

i.e., $F = W \oplus S_1 \oplus S_2$

02. Ans: 195

Sol: In a 16 bit parallel binary adder, the carry has to propagate 15 stages plus the maximum of time taken for producing sum and carry worst case Delay, T = 15×12+15

T = 180+15

T = 195 ns

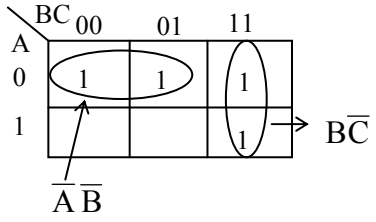
03. Ans. (d)

Sol: The given circuit is binary parallel adder/subtractor circuit. It performs A+B, A–B and A+1 operations.

K	C_0	B	Operation
0	0	B	A+B (addition)
0	1	B	A+B+1(addition with carry)
0	1	0	A+1(increment)
1	0	B	A+ B(1's complement addition)
1	1	B	A+B+1(2's complement subtraction)
1	0	0	A–1(decrement)

04 Ans: (c)

Sol: $Z(A, B, C) = \Sigma m(0,1,2,6) + \overline{C}$



Hence $Z = \overline{C} + \left(\overline{A}\,\overline{B} + B\overline{C}\right)$

$\Rightarrow \quad Z = \overline{A}\,\overline{B} + \overline{C}$

05. Ans: 6

Sol: T = 0 → NOR → MUX 1 → MUX 2

2ns 1.5ns 1.5ns

Delay = 2ns + 1.5ns + 1.5ns = 5ns

T = 1→ NOT→MUX 1 → NOR → MUX 2

1ns 1.5ns 2ns 1.5ns

Delay = 1 ns + 1.5 ns + 2 ns + 1.5 ns = 6 ns

Hence, the maximum delay of the circuit is 6 ns

06. Ans: –1

Sol: When all bits in 'B' register is '1', then only it gives highest delay.

∴ '–1' in 8 bit notation of 2's complement is 1111 1111

07. Ans: (c)

Sol: 4 × 1 MUX having only 2-select lines so implement all 2-variable functions and some of 3- variable functions also possible.

08. Ans: (b)

Sol: Subtraction of Two numbers

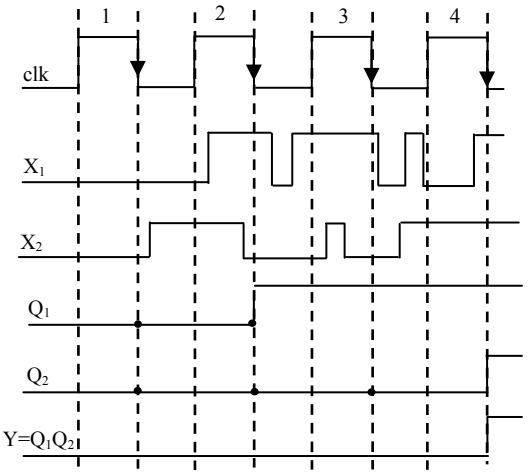
5. Sequential Circuits

01. Ans: (c)

Sol: Given Clk, X_1, X_2

Output of First D-FF is Q_1

Output of Second D-FF is Q_2



02. Ans: (d)

Sol:

Q_2	Q_1	Q_{2N}	Q_{1N}	T_1
0	1	1	0	0
0	1	0	0	1
1	0	1	1	1
1	1	0	1	0

$T_1 = \overline{Q}_2 Q_1 + Q_2 \overline{Q}_1 = Q_1 \oplus Q_2$

03. Ans: (b)

04. Ans: (d)

05. Ans: 4

Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

06. Ans: 3

Sol:

$0 \rightarrow 0\ 0$

$0 \rightarrow 0\ 0$

$1 \rightarrow 0\ 1$

$1 \rightarrow 0\ 1$

$2 \rightarrow 1\ 0$

$2 \rightarrow 1\ 0$

$3 \rightarrow 1\ 1$

$3 \rightarrow 1\ 1$

To avoid Repetition it requires one extra bit.

07. Ans: (b)

Sol:

CLK	Serial in $= B \oplus C \oplus D$	A	B	C	D
0		1	0	1	0
1	$1 \rightarrow$	1	1	0	1
2	$0 \rightarrow$	0	1	1	0
3	$0 \rightarrow$	0	0	1	1
4	$0 \rightarrow$	0	0	0	1
5	$1 \rightarrow$	1	0	0	0
6	$0 \rightarrow$	0	1	0	0
7	$1 \rightarrow$	1	0	1	0

08. Ans: (b)

Sol:

J	K	Q_n	$\overline{Q}_n$	$T = (J + Q_n)$ $(K + \overline{Q}_n)$	Q_{n+1}
0	0	0	1	0.1 = 0	0
0	0	1	0	1.0 = 0	1 Q_n
0	1	0	1	0.1 = 0	0
0	1	1	0	1.1 = 1	0 0
1	0	0	1	1.1 = 1	1
1	0	1	0	1.0 = 0	1 1
1	1	0	1	1.1 = 1	1
1	1	1	0	1.1 = 1	0 $\overline{Q}_n$

09. Ans: (a)

Sol: $Q_3\ Q_2\ Q_1\ Q_0 = (1\quad 1\quad 0\quad 0)$

Output NAND GATE is 0

It is a mod 12 counter

$\therefore$ Frequency of O/P $= \frac{10\,\text{KHz}}{12}$

$= 0.833$ KHz

10. Ans: (c)

Sol: D-FF characteristic equation is

$Q(t+1) = D \rightarrow (1)$

But given $D = X \oplus Q(t)$

Hence $(1) \rightarrow Q(t+1) = x \oplus Q(t) \rightarrow (2)$

Eq (2) resembles characteristic equation of T-FF

11. Ans: 7

Sol: The counter is cleared when

$Q_DQ_CQ_BQ_A = 0110$

Clk	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	0	0

As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get's cleared during the 7^{th} clock pulse.

$\therefore$ mod of counter = 7

12. Ans: (c)

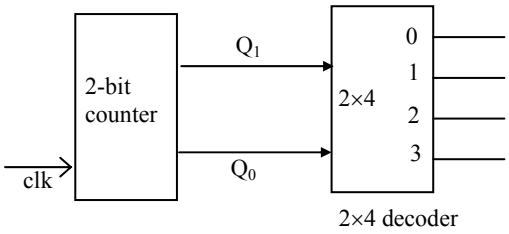
Sol: State table for the given state diagram

State	Input	Output	Next state
S_0	0	1	S_0
S_0	1	0	S_1
S_1	0	1	S_0
S_1	1	0	S_1

Output is 1's complement of a binary input.

13. Ans: (c)

Sol: Assume n = 2



2×4 decoder

Outputs of counter is connected to inputs of decoder

Counter outputs		Decoder inputs		Decoder outputs			
Q_1	Q_0	a	b	d_3	d_2	d_1	d_0
0	0	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0

The overall circuit acts as 4-bit ring counter

n = 2

$\therefore$ k = 2^2 = 4 k-bit ring counter

Additional Questions

Number Systems

01. Ans: (d)

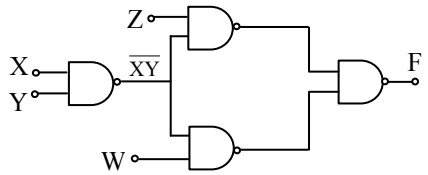
02. Ans: (d)

Sol: $(8 \times 7 + 3)_{10} = (11 \times 5 + 4)_{10}$

Logic Gates & Boolean Algebra

03. Ans: (b)

Sol: $F = (\overline{X} + \overline{Y})(Z+W) = \overline{XY}Z + \overline{XY}W$



$\therefore$ Number of NAND gates required are 4

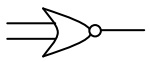
04. Ans: (a)

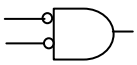
Sol: Given: $A + A\overline{B} + A\overline{B}C$

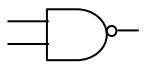
$= A[1 + \overline{B} + \overline{B}C] = A$

Not even single NAND GATE is required to implement A.

05. Ans: (d)

Sol: P.  $\overline{A+B}$

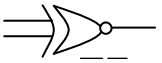
4.  $\overline{A}.\overline{B} = \overline{A+B}$

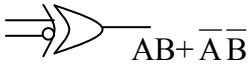
Q.  $\overline{A.B}$

2.  $\overline{A} + \overline{B} = \overline{A.B}$

R.  $\overline{A}B + A\overline{B}$

3.  $\overline{A}B + A\overline{B}$

S.  $AB + \overline{A}\,\overline{B}$

1.  $AB + \overline{A}\,\overline{B}$

06. Ans: (a)

Sol: Coincidence logic is XNOR logic.

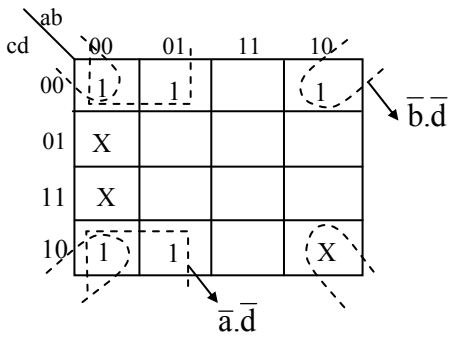
Among all the options, option (a) represents

$F = xy + \overline{x}\,\overline{y}$ = coincidence logic.

K-Maps

07. Ans: (a)

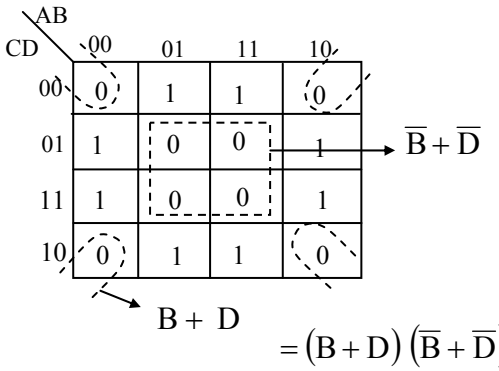
Sol: Quad: $\overline{a}\,\overline{d}$, Quad : $\overline{b}\,\overline{d}$



$= \overline{a}.\overline{d} + \overline{b}.\overline{d}$

08. Ans: (c)

Sol:



$= (B + D)(\overline{B} + \overline{D})$

09. Ans: (c)

Sol: $f = \overline{A}B\overline{C} + \overline{A}\,\overline{B}\,C + ABC + A\overline{B}\overline{C}$

$= (\overline{A}B + A\overline{B})\overline{C} + (AB + \overline{A}\overline{B})C$

$= (A \oplus B)\overline{C} + (A \odot B)\,C = A \oplus B \oplus C$

Combinational Circuits

10. Ans: (a)

Sol:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

i.e., $F(A,B,C) = \sum m(1,2,4,6)$

	I_0	I_1	I_2	I_3
$\overline{A}$	0	①	②	3
A	④	5	⑥	7

11. Ans: (a)

Sol: Output: f(x,y,z)

z = 0 the only MUX get ends

Characteristic Exp:

$E_N\left(\overline{A}_1\,\overline{A}_0 \,.\, I_0 + \overline{A}_1 A_0 \,.\, I_2 + A_1\,\overline{A}_0 \,.\, I_2 + A_1 A_0 I_3\right)$

$= z^1\,\left((y^1)\right)^1 .\; z^1 \,.\, x + \left((y^1)\right)^1 .\; z \,.\, x + y^1$

$z^1 \,.\, y + y^1 z \,.\, y^1$

$= z^1 \,.\, x.y \;+\; \underline{z^1 \,.\, z\; y}x \;+\; \underline{z^1 . x^1 . y} +$

$\underline{z^1 \,.\, z^1 . y^1}$

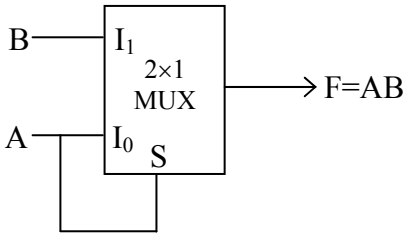
$= x\,y\,z^1$

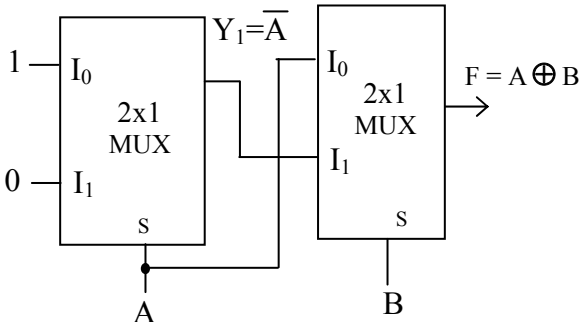
12. Ans: (a)

Sol: $F = \overline{S}\,I_0 + SI_1$

$= \overline{A}.A + A\,B = AB$

= AND gate





$F = A\overline{B} + \overline{A}B$

$= A \oplus B$ = EX-OR Gate

To realize 2 Input AND gate and 2 Input EX-OR gate the no. of 2 × 1 MUX required are 1 and 2 respectively.

13. Ans: (a)

Sol: As per the definition of MUX output equation is

$F = \overline{S}_1\overline{S_0}\ I_0 + \overline{S_1}S_0I_1 + S_1\overline{S_0}\ I_2 + S_1S_0I_3$

$I_0 = 0; \qquad I_1 = 1;$

$I_2 = R; \qquad I_3 = \overline{R};\ S_0 = Q;\ S_1 = P$

$\therefore F = \overline{P}\ \overline{Q}.0 + \overline{P}Q.1 + P\overline{Q}.R + PQ\overline{R}$

$= \overline{P}Q + P\overline{Q}R + PQ\overline{R}$

$= \overline{P}QR + \overline{P}Q\overline{R} + P\overline{Q}R + PQ\overline{R}$

$= \Sigma m(2,3,5,6) = \overline{P}Q + Q\overline{R} + P\overline{Q}R$

Sequential Circuits

14. Ans: (c)

Sol: From the given figure:

$J_0 = \overline{Q}_1$; $J_1 = Q_0$; $K_0 = K_1 = 1$.

CLK	Q_1	Q_0	$J_0 = \overline{Q}_1$, $K_0=1$		$J_1=Q_0$, $K_1=1$	
1	0	0	1	1	0	1
2	0	1	1	1	1	1
3	1	0	0	1	0	1
	0	0				

Counter is coming to initial state after 3clock pulses. Hence K = 3

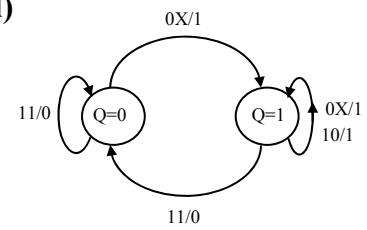
15. Ans: (c)

Sol: The clear I/P should be Active Low i.e., 2 input gate o/p should be Low. $\overline{C}$ & $\overline{B}$ are the inputs of the 2 input OR gate

(OR gate output $\overline{C} + \overline{B} = \overline{CB}$)

16. Ans: (d)

Sol:



Initial output = 0
let a, b inputs

a	b	Q
1	1	0
0	X	1
1	0	1

Initial output Q = 1

a	b	Q
1	1	0
0	X	1
1	0	1

a	b	Q
0	0	1
0	1	1
1	0	1
1	1	0

It is a NAND gate