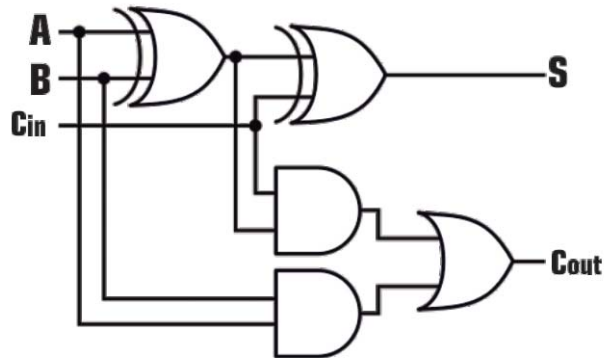




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INSTRUMENTATION ENGINEERING

DIGITAL ELECTRONICS & MICROPROCESSORS

Volume-1 : Study Material with Classroom Practice Questions

01. Ans: (d)**Sol:** $135_x + 144_x = 323_x$

$$(1 \times x^2 + 3 \times x^1 + 5 \times x^0) + (1 \times x^2 + 4 \times x^1 + 4 \times x^0) = 3x^2 + 2x^1 + 3x^0$$

$$\Rightarrow x^2 + 3x + 5 + x^2 + 4x + 4 = 3x^2 + 2x + 3$$

$$x^2 - 5x - 6 = 0$$

$$(x-6)(x+1) = 0 \quad (\text{Base cannot be negative})$$

Hence $x = 6$.

(OR)

As per the given number x must be greater than 5. Let consider $x = 6$

$$(135)_6 = (59)_{10}$$

$$(144)_6 = (64)_{10}$$

$$(323)_6 = (123)_{10}$$

$$(59)_{10} + (64)_{10} = (123)_{10}$$

So that $x = 6$ **02. Ans: (a)****Sol:** 8-bit representation of

$$+127_{10} = 01111111_{(2)}$$

1's complement representation of

$$-127 = 10000000.$$

2's complement representation of

$$-127 = 10000001.$$

No. of 1's in 2's complement of

$$-127 = m = 2$$

No. of 1's in 1's complement of

$$-127 = n = 1$$

$$\therefore m:n = 2:1$$

03. Ans: (c)**Sol:** In 2's complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is ' X_3 ', hence it can be extended left any number of times.**04. Ans: (c)****Sol:** Binary representation of $+(539)_{10}$:

$$\begin{array}{r} 2 \overline{) 539} \\ 2 \overline{) 269} -1 \\ 2 \overline{) 134} -1 \\ 2 \overline{) 67} -0 \\ 2 \overline{) 33} -1 \\ 2 \overline{) 16} -1 \\ 2 \overline{) 8} -0 \\ 2 \overline{) 4} -0 \\ 2 \overline{) 2} -0 \\ 1 -0 \end{array}$$

$$(+539)_{10} = (10000 \ 11 \ 0 \ 11)_2 = (00100 \ 0011011)_2$$

$$2'S \text{ complement} \rightarrow 110111100101$$

$$\text{Hexadecimal equivalent} \rightarrow (DE5)_H$$

05. Ans: 5**Sol:** Symbols used in this equation are 0,1,2,3
Hence base or radix can be 4 or higher

$$(312)_x = (20)_x (13.1)_x$$

$$3x^2 + 1x + 2x^0 = (2x+0)(x+3x^0+x^{-1})$$

$$3x^2 + x + 2 = (2x) \left(x + 3 + \frac{1}{x} \right)$$

$$3x^2 + x + 2 = 2x^2 + 6x + 2$$

$$x^2 - 5x = 0$$

$$x(x-5) = 0$$

$$x = 0(\text{or}) x = 5$$

$$x \text{ must be } x > 3, \text{ So } x = 5$$



06. Ans: 3

Sol: $123_5 = x8_y$

$$1 \times 5^2 + 2 \times 5^1 + 3 \times 5^0 = x.y^1 + 8 \times y^0$$

$$25 + 10 + 3 = xy + 8$$

$$\therefore xy = 30$$

Possible solutions:

i. $x = 1, y = 30$

ii. $x = 2, y = 15$

iii. $x = 3, y = 10$

\therefore 3 possible solutions exists.

07. Ans: 1

Sol: The range (or) distinct values

$$\text{For 2's complement} \Rightarrow -(2^{n-1}) \text{ to } +(2^{n-1}-1)$$

For sign magnitude

$$\Rightarrow -(2^{n-1}-1) \text{ to } +(2^{n-1}-1)$$

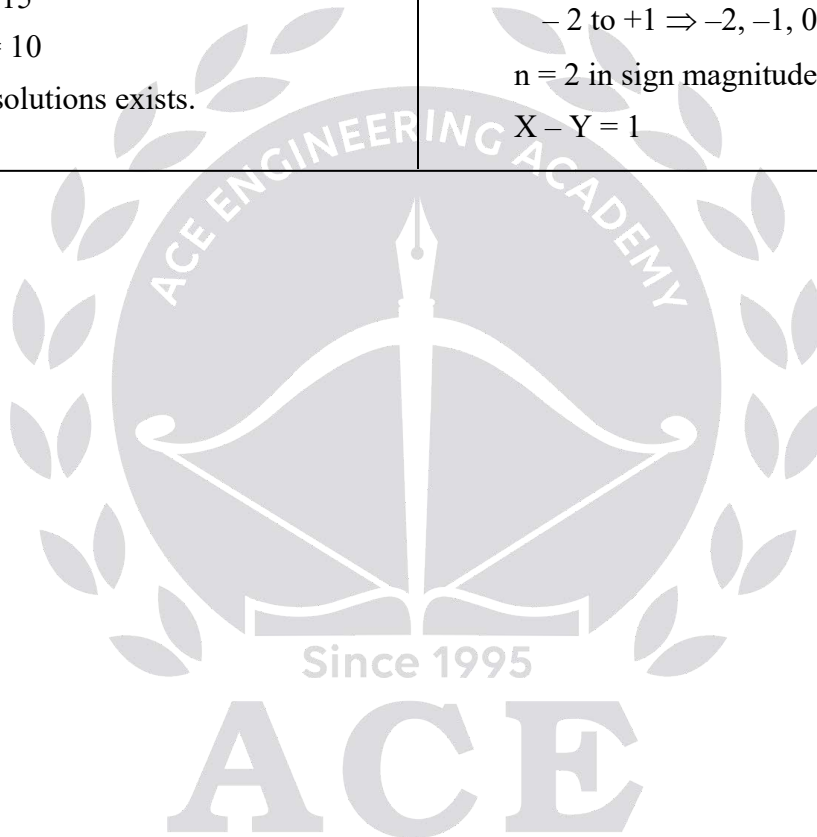
Let $n = 2 \Rightarrow$ in 2's complement

$$-(2^{2-1}) \text{ to } +(2^{2-1}-1)$$

$$-2 \text{ to } +1 \Rightarrow -2, -1, 0, +1 \Rightarrow X = 4$$

$$n = 2 \text{ in sign magnitude} \Rightarrow -1 \text{ to } +1 \Rightarrow Y = 3$$

$$X - Y = 1$$



01. Ans: (c)

Sol: Given 2's complement numbers of sign bits are x & y . z is the sign bit obtained by adding above two numbers. \therefore Overflow is indicated by $= \bar{x}\bar{y}z + x y \bar{z}$

Examples

1. $A = +7$ 0111
 $B = +7$ 0111
 14 1110 $\Rightarrow \bar{x}\bar{y}z$
2. $A = +7$ 0111
 $B = +5$ 0101
 12 1100 $\Rightarrow \bar{x}\bar{y}z$
3. $A = -7$ 1001
 $B = -7$ 1001
 -14 10010 $\Rightarrow x y \bar{z}$
4. $A = -7$ 1001
 $B = -5$ 1011
 -12 10100 $\Rightarrow x y \bar{z}$

02. Ans: (b)

Sol: Truth table of XOR

A	B	o/p
0	0	0
0	1	1
1	0	1
1	1	0

Stage 1:

Given one i/p = 1 Always.

1	X	o/p	
1	0	1	$= \bar{X}$
1	1	0	$= X$

For First XOR gate o/p = \bar{X}

Stage 2:

\bar{X}	X	o/p
0	1	1
1	0	1

For second XOR gate o/p = 1.

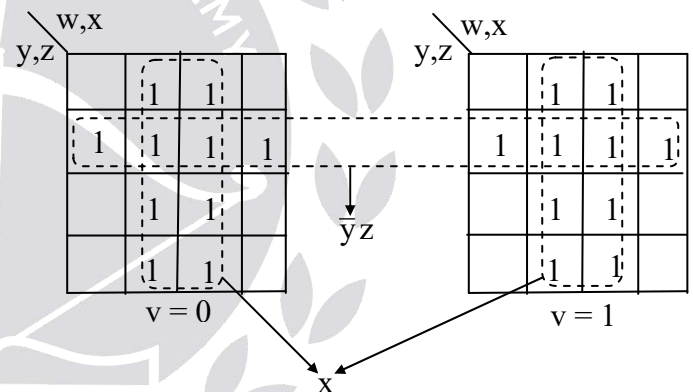
Similarly for third XOR gate o/p = \bar{X} & for fourth o/p = 1

For Even number of XOR gates o/p = 1

For 20 XOR gates cascaded o/p = 1.

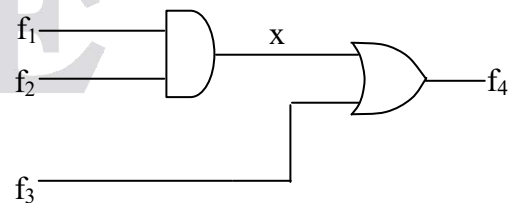
03. Ans: (b)

Sol:



04. Ans: (c)

Sol:

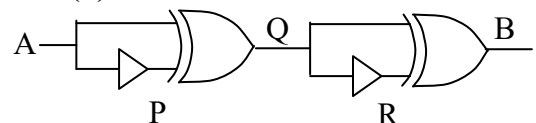


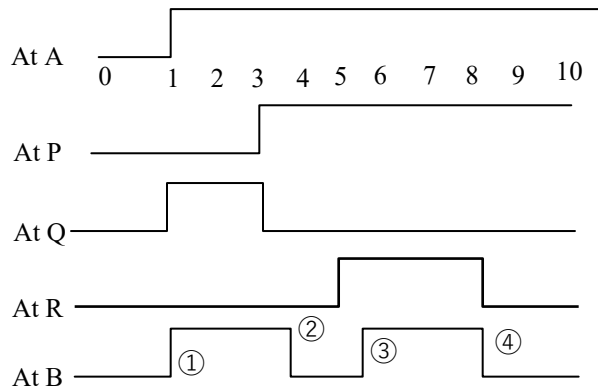
$$x = f_1 f_2$$

$$f_4 = f_1 \cdot f_2 + f_3$$

05. Ans: (d)

Sol:





06. Ans: (c)

Sol: $\overline{x_1} \oplus \overline{x_3} = \overline{x_1} x_3 + x_1 \overline{x_3} = y$

$\overline{x_2} \oplus \overline{x_4} = \overline{x_2} x_4 + x_2 \overline{x_4} = z$

$(\overline{x_1} \oplus \overline{x_3}) \oplus (\overline{x_2} \oplus \overline{x_4})$

$= y \oplus z = 0, \text{ when } y = z$

\therefore option (c) is true

For all cases option A, B, D not satisfy.

07. Ans: (b)

Sol: $M(a,b,c) = ab + bc + ca$

$\overline{M(a,b,c)} = \overline{bc} + \overline{ab} + \overline{ac}$

$M(a,b,\overline{c}) = ab + b\overline{c} + \overline{c}a$

$M(\overline{M(a,b,c)}, M(a,b,\overline{c}), c)$

$= (\overline{bc} + \overline{ab} + \overline{ac})(ab + b\overline{c} + \overline{c}a)$
 $+ (ab + b\overline{c} + \overline{c}a)c + (\overline{bc} + \overline{ab} + \overline{ac})c$

$= (\overline{bc} + \overline{ab} + \overline{ac})(ab + b\overline{c} + \overline{c}a)$
 $+ (\overline{bc} + \overline{ab} + \overline{ac})c + abc$

$= \overline{ab}\overline{c} + \overline{ab}c + abc + \overline{a}b\overline{c}$

$= \overline{c}[a\overline{b} + \overline{a}b] + c[ab + \overline{a}b]$

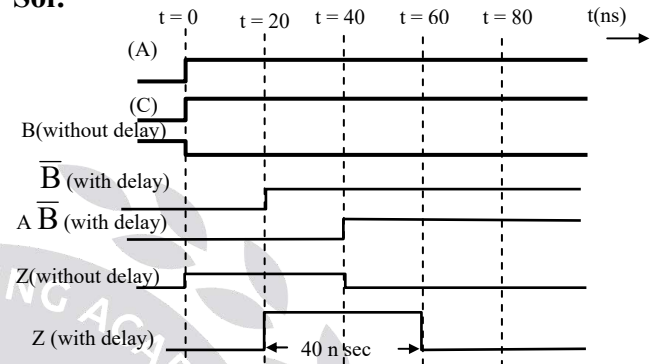
$= \sum m(1, 2, 4, 7)$

$\therefore M(x, y, z) = a \oplus b \oplus c$

Where $x = \overline{M(a,b,c)}, y = M(a,b,\overline{c}), z = c$

08. Ans: 40

Sol:



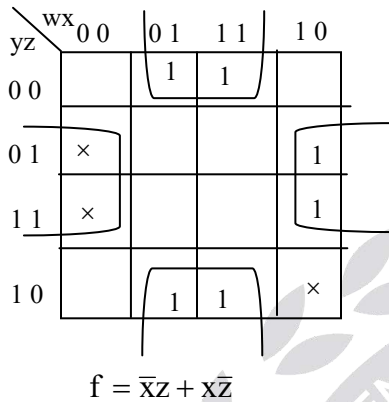
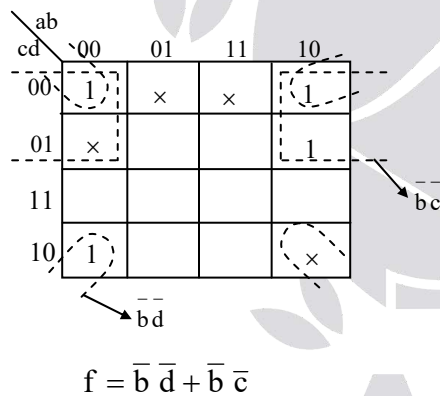
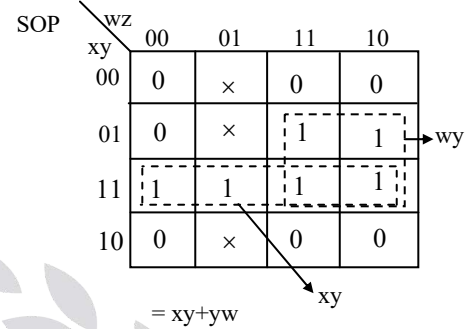
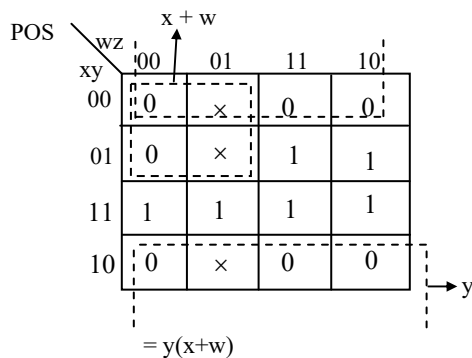
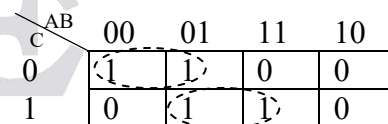
$\therefore Z$ is 1 for 40 nsec

09. Ans: (c)

Sol: Logic gates $\overline{X} + Y = \overline{X\overline{Y}} = \overline{XY_1}$

Where $Y_1 = \overline{Y}$

It is a NAND gate and thus the gate is 'Universal gate'.

01. Ans: (b)**Sol:****02. Ans: (b)****Sol:****03.****Sol:****SOP:** $x y + y w$ **POS:** $y(x + w)$ **04. Ans: (a)****Sol:** For n-variable Boolean expression,Maximum number of minterms = 2^n Maximum number of implicants = 2^n Maximum number of prime implicants = $\frac{2^n}{2}$ $= 2^{n-1}$ **05. Ans: (c)****Sol:****F(A, B, C) = $\bar{A}\bar{C} + BC$** **06. Ans: 1****Sol:** After minimization = $(\bar{A} + \bar{B} + \bar{C} + \bar{D})$ $= ABCD$ \therefore only one minterm.



07. Ans: 3

Sol: $\bar{w}\bar{z} + \bar{w}xy + \bar{x}y\bar{z}$

		yz			
		00	01	11	10
wx	00	1			1
	01	1	1		1
	11				
	10				1



01. Ans: (d)

Sol: Let the output of first MUX is “ F_1 ”

$$F_1 = AI_0 + AI_1$$

Where A is selection line, I_0, I_1 = MUX Inputs

$$F_1 = \bar{S}_1 \cdot W + S_1 \cdot \bar{W} = S_1 \oplus W$$

Output of second MUX is

$$F = \bar{A} \cdot I_0 + A \cdot I_1$$

$$F = \bar{S}_2 \cdot F_1 + S_2 \cdot \bar{F}_1$$

$$F = S_2 \oplus F_1$$

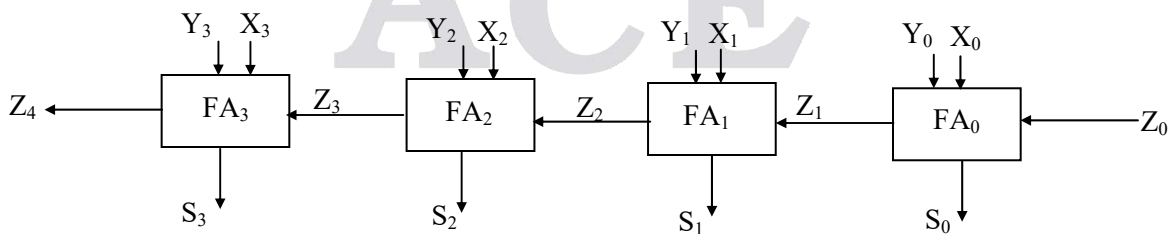
$$\text{But } F_1 = S_1 \oplus W$$

$$F = S_2 \oplus S_1 \oplus W$$

$$\text{i.e., } F = W \oplus S_1 \oplus S_2$$

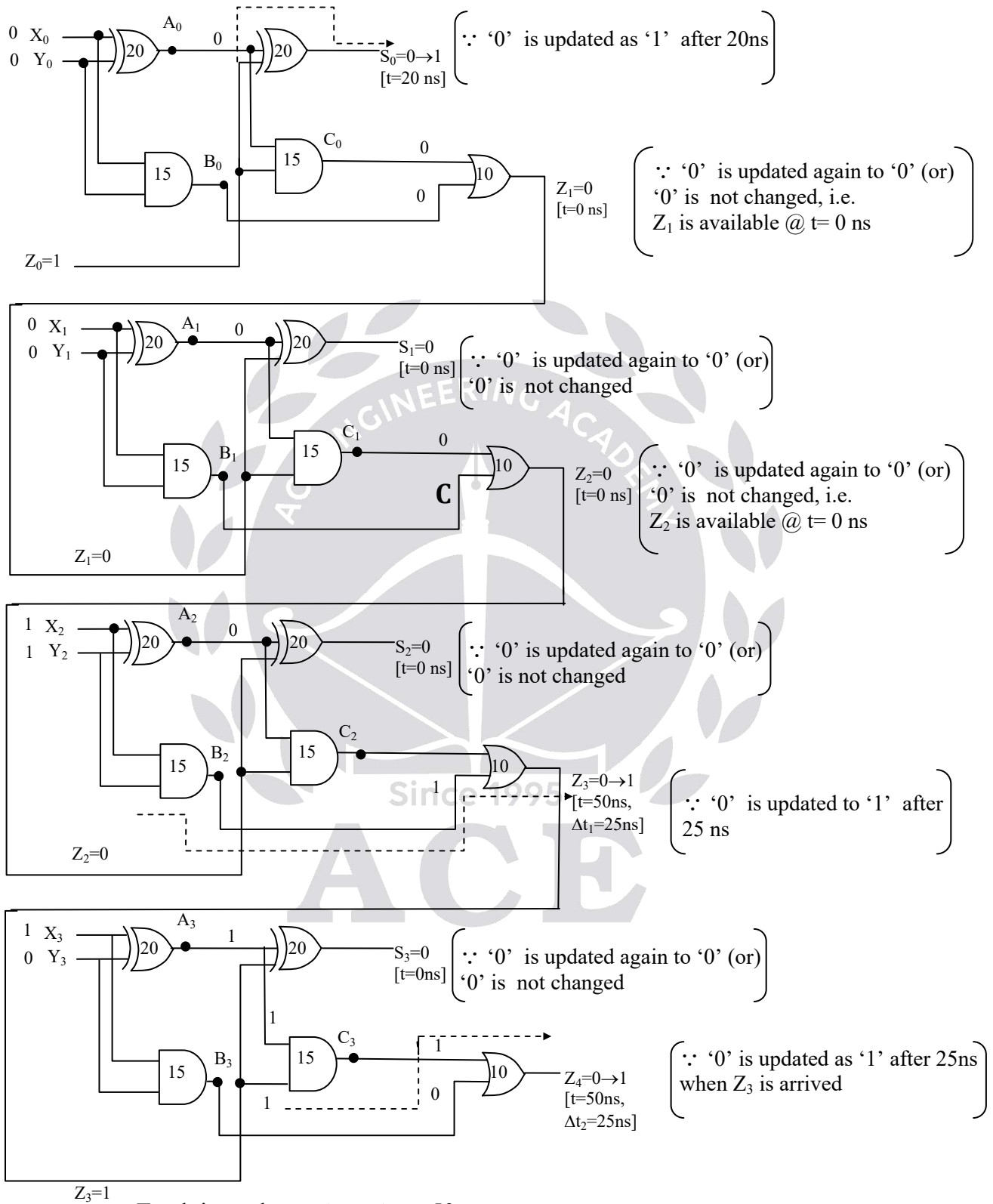
02. Ans: 50

Sol:



Initially all the output values are ‘0’, at $t = 0$, the inputs to the 4-bit adder are changed to $X_3X_2X_1X_0 = 1100$, $Y_3Y_2Y_1Y_0 = 0100$

----- indicates critical path delay to get the output





03. Ans: (a)

Sol: The given circuit is binary parallel adder/subtractor circuit. It performs $A+B$, $A-B$ but not $A + 1$ operations.

K	C ₀	Operation
0	0	$A+B$ (addition)
0	1	$A+B+1$ (addition with carry)
1	0	$A+\overline{B}$ (1's complement addition)
1	1	$A+\overline{B}+1$ (2's complement subtraction)

04. Ans: (d)

Sol: It is expansion of 2:4 decoders to 1:8 demultiplexer A_1, A_0 must be connected to S_1, S_0 i.e.,
 $R = S_0, S = S_1$

Q must be connected to S_2 i.e., $Q = S_2$

P is serial input must be connected to D_{in}

05. Ans: 6

Sol: $T = 0 \rightarrow \text{NOR} \rightarrow \text{MUX 1} \rightarrow \text{MUX 2}$
 2ns 1.5ns 1.5ns

Delay = $2\text{ns} + 1.5\text{ns} + 1.5\text{ns} = 5\text{ns}$

$T = 1 \rightarrow \text{NOT} \rightarrow \text{MUX 1} \rightarrow \text{NOR} \rightarrow \text{MUX 2}$
 1ns 1.5ns 2ns 1.5ns

Delay = $1\text{ns} + 1.5\text{ns} + 2\text{ns} + 1.5\text{ns} = 6\text{ns}$

Hence, the maximum delay of the circuit is 6ns

06. Ans: -1

Sol: When all bits in 'B' register is '1', then only it gives highest delay.

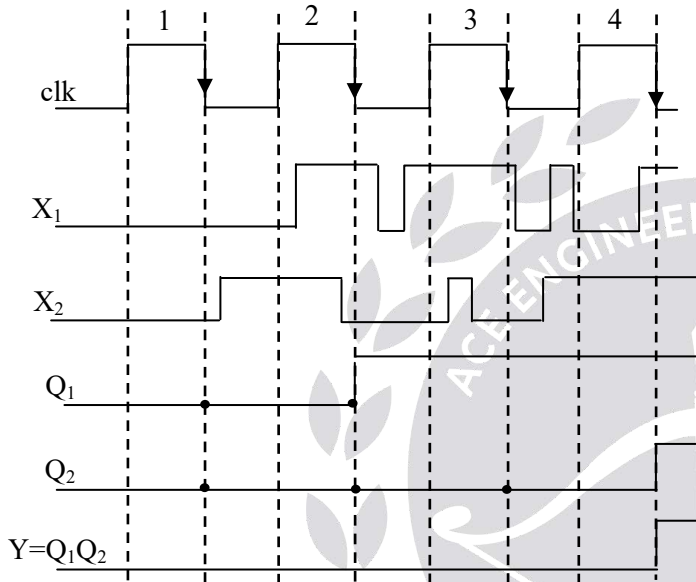
\therefore '-1' in 8 bit notation of 2's complement is 1111 1111

01. Ans: (c)

Sol: Given Clk, X_1 , X_2

Output of First D-FF is Q_1

Output of Second D-FF is Q_2



02. Ans: 4

Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

03. Ans: 7

Sol: The counter is cleared when $Q_D Q_C Q_B Q_A = 0110$

Clk	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	0	0

As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get's cleared during the 7th clock pulse.

\therefore mod of counter = 7

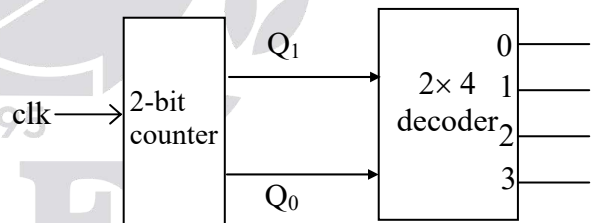
04. Ans: (b)

Sol: The given circuit is a mod 4 ripple down counter. Q_1 is coming to 1 after the delay of $2\Delta t$.

CLK	Q_1	Q_0
	0	0
1	1	1
2	1	0
3	0	1
4	0	0

05. Ans: (c)

Sol: Assume $n = 2$



Outputs of counter is connected to inputs of decoder

Counter outputs		Decoder inputs		Decoder outputs			
Q_1	Q_0	a	b	d_3	d_2	d_1	d_0
0	0	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0

The overall circuit acts as 4-bit ring counter $n = 2$

$\therefore k = 2^2 = 4$, k-bit ring counter



06. Ans: (b)

Sol:

CLK	Serial in= $B \oplus C \oplus D$	A B C D
0		1 0 1 0
1	1 \longrightarrow	1 1 0 1
2	0 \longrightarrow	0 1 1 0
3	0 \longrightarrow	0 0 1 1
4	0 \longrightarrow	0 0 0 1
5	1 \longrightarrow	1 0 0 0
6	0 \longrightarrow	0 1 0 0
7	1 \longrightarrow	1 0 1 0

\therefore After 7 clock pulses content of shift register become 1010 again

07. Ans: (b)

Sol:

J	K	Q	\bar{Q}_n	$T = (J + Q_n)(K + \bar{Q}_n)$	Q_{n+1}
0	0	0	1	$0.1 = 0$	0
0	0	1	0	$1.0 = 0$	1
0	1	0	1	$0.1 = 0$	0
0	1	1	0	$1.1 = 1$	0
1	0	0	1	$1.1 = 1$	1
1	0	1	0	$1.0 = 0$	1
1	1	0	1	$1.1 = 1$	1
1	1	1	0	$1.1 = 1$	0

J \ K	00	01	11	10
0			1	
1	1		1	1

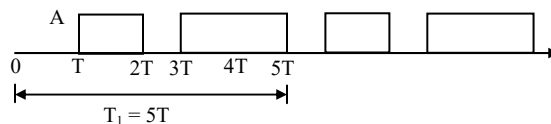
$$T = J \bar{Q}_n + K Q_n = (J + Q_n)(K + \bar{Q}_n)$$

08. Ans: 1.5

Sol:

C/k	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Y = Q ₃ + Q ₅
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0

The waveform at OR gate output, Y is [A = +5V]



Average power

$$P = \frac{V_{Ao}^2}{R} = \frac{1}{R} \left[\lim_{T_1 \rightarrow \infty} \frac{1}{T_1} \int_0^{T_1} y^2(t) dt \right] = \frac{1}{RT_1} \left[\int_T^{2T} A^2 dt + \int_{3T}^{4T} A^2 dt \right]$$

$$= \frac{A^2}{RT_1} [(2T - T) + (4T - 3T)] = \frac{A^2 \cdot 3T}{R(5T)} = \frac{5^2 \cdot 3}{10 \times 5} = 1.5 \text{ mw}$$



09. Ans: (b)

Sol:

Present State	Next State		Output (Y)	
	X = 0	X = 1	X = 0	X = 1
A	A	E	0	0
B	C	A	1	0
C	B	A	1	0
D	A	B	0	1
E	A	C	0	1

Step (1):

By replacing state B as state C then state B, C are equal.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
B	B	A
D	A	B
E	A	B

Step (2):

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	E
B	B	A
D	A	B
E	A	B

State D, E are equal, remove state E and replace E with D in next state.

Reducing state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B
D	A	B

Finally reduced state table is

Reduced state table		
Present state	Next state	
	X = 0	X = 1
A	A	D
B	B	A
D	A	B

∴ 3 states are present in the reduced state table

10. Ans: (c)

Sol: State table for the given state diagram

State	Input	Output
S ₀	0	1
S ₀	1	0
S ₁	0	1
S ₁	1	0

Output is 1's complement of input.

11. Ans: (c)

Sol: In state (C), when XYZ = 111, then Ambiguity occurs
Because, from state (C)
⇒ When X = 1, Z = 1
⇒ N.S is (A)
When Y = 1, Z = 1 ⇒ N.S is (B)

6

Logic Gate Families

Chapter

01. Ans: (v)

Sol: $V_{OH}(\min)$:-

(High level output voltage)

The minimum voltage level at a Logic circuit output in the logic '1' state under defined load conditions.

$V_{OL}(\max)$:-

(Low level output voltage)

The maximum voltage level at a logic circuit output in the Logical '0' state under defined load conditions.

$V_{IL}(\max)$:- (Low level input voltage)

The maximum voltage level required for a logic '0' at an input. Any voltage above this level will not be accepted as a Low by the logic circuit.

$V_{IH}(\min)$:- (High level Input voltage)

The minimum voltage level required for logic '1' at an input. Any voltage below this level will not be accepted as a HIGH by the Logic circuit.

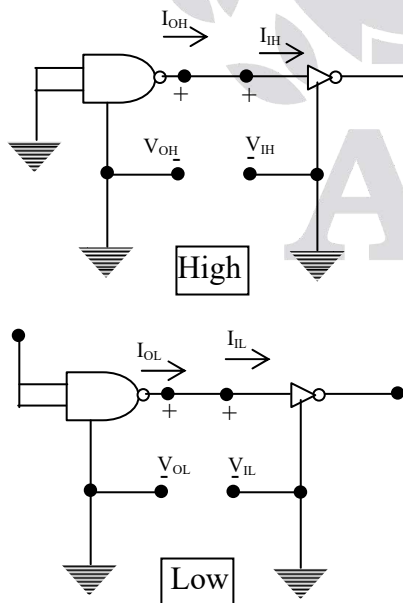


Fig: currents and voltages in the two logic states.

02. Ans: (b)

Sol: Fan out is minimum in DTL

(High Fan-out = CMOS)

Power consumption is minimum in CMOS.
Propagation delay is minimum in ECL
(fastest = ECL)

03. Ans: (b)

Sol: When $V_1 = 2.5V$,

Q_1 is in reverse active region

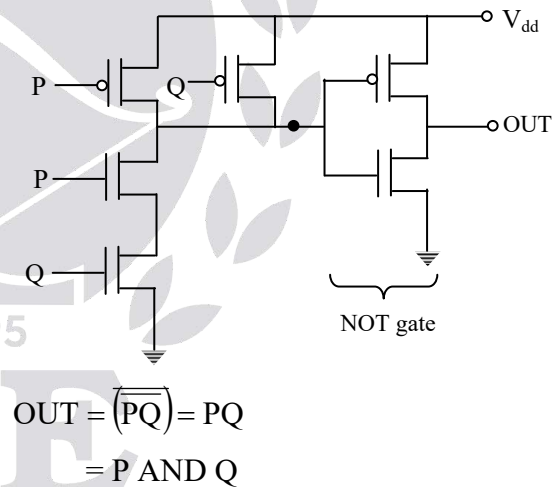
Q_2 is in saturation region

Q_3 is in saturation region

Q_4 is in cut-off region

04. Ans: (d)

Sol: The given circuit can be redrawn as below:



05. Ans: (b)

Sol: As per the description of the question, when the transistor Q_1 and diode both are OFF then only output $z = 1$.

X	Y	Z	Remarks
0	0	0	Q_1 is OFF, Diode is ON
0	1	1	Q_1 is OFF, Diode is OFF
1	0	0	Q_1 is ON, Diode is OFF
1	1	0	Q_1 is ON, Diode is OFF

Hence $Z = \overline{XY}$

7

A/D & D/A Converters

Chapter

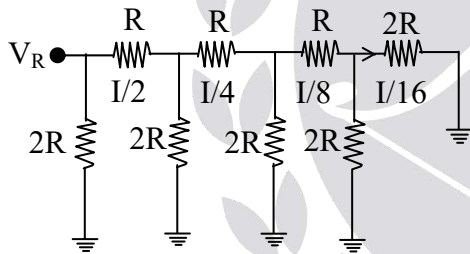
01. Ans: (b)

Sol:

CLK	Counter			Decoder				V ₀
	Q ₂	Q ₁	Q ₀	D ₃	D ₂	D ₁	D ₀	
1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1	1
3	0	1	0	0	0	1	0	2
4	0	1	1	0	0	1	1	3
5	1	0	0	1	0	0	0	8
6	1	0	1	1	0	0	1	9
7	1	1	0	1	0	1	0	10
8	1	1	1	1	0	1	1	11

02. Ans: (b)

Sol:



$$R_{\text{equ}} = (((((2R \parallel 2R) + R) \parallel 2R) + R) \parallel 2R) + R \parallel 2R$$

$$R_{\text{equ}} = R = 10k\Omega$$

$$I = \frac{V_R}{R} = \frac{10V}{10k} = 1mA$$

$$\text{Current division at } \frac{I}{16} = \frac{1 \times 10^{-3}}{16} = 62.5 \mu A$$

03. Ans: (c)

Sol: Net current at inverting terminal,

$$I_i = \frac{I}{4} + \frac{I}{16} = \frac{5I}{16}$$

$$V_0 = -I_i R = -\frac{5I}{16} \times 10k\Omega = \frac{-5 \times 1 \times 10^{-3} \times 10 \times 10^3}{16} = -3.125V$$

04. Ans: (d)

Sol: Given that $V_{\text{DAC}} = \sum_{n=0}^3 2^{n-1} b_n$ Volts

$$V_{\text{DAC}} = 2^{-1} b_0 + 2^0 b_1 + 2^1 b_2 + 2^2 b_3$$

$$\Rightarrow V_{\text{DAC}} = 0.5b_0 + b_1 + 2b_2 + 4b_3$$

Initially counter is in 0000 state

Up counter o/p		V _{DAC} (V)	o/p of comparator
b ₃	b ₂ b ₁ b ₀		
0	0 0 0	0	1
0	0 0 1	0.5	1
0	0 1 0	1	1
0	0 1 1	1.5	1
0	1 0 0	2	1
0	1 0 1	2.5	1
0	1 1 0	3	1
0	1 1 1	3.5	1
1	0 0 0	4	1
1	0 0 1	4.5	1
1	0 1 0	5	1
1	0 1 1	5.5	1
1	1 0 0	6	1
1	1 0 1	6.5	0

When $V_{\text{DAC}} = 6.5$ V, the o/p of comparator is '0'. At this instant, the clock pulses to the counter are stopped and the counter remains in 1101 state.

\therefore The stable reading of the LED display is 13.



05. Ans: (b)

Sol: The magnitude of error between V_{DAC} & V_{in} at steady state is $|V_{DAC} - V_{in}| = |6.5 - 6.2|$
 $= 0.3 \text{ V}$

06. Ans: (a)

Sol: In Dual slope

$$ADC \Rightarrow V_{in} T_1 = V_R \cdot T_2$$

$$\Rightarrow V_{in} = \frac{V_R T_2}{T_1}$$

$$= \frac{100 \text{ mV} \times 370.2 \text{ ms}}{300 \text{ ms}}$$

DVM indicates = 123.4

07. Ans: (d)

Sol: Ex: $f_{in} = 1 \text{ kHz} \rightarrow f_s = 2 \text{ kHz}$

$$f_{in} = 25 \text{ kHz} \leftarrow f_s = 50 \text{ kHz}$$

$$1. \text{ Max conversion time} = 2^{N+1} T = 2^{11} \cdot 1 \mu\text{s}$$

$$= 2048 \mu\text{s}$$

$$2. \text{ Sampling period} = T_s \geq \text{maximum conversion time}$$

$$T_s \geq 2048 \mu\text{s}$$

$$3. \text{ Sampling rate } f_s = \frac{1}{T_s} \leq \frac{1}{2048 \times 10^{-6}}$$

$$f_s \leq 488 \quad f_s \leq 500 \text{ Hz}$$

$$4. f_{in} = \frac{f_s}{2} = 250 \text{ Hz}$$

01. Ans: (a)

Sol: chip select is an active low signal for $\text{chipselect} = 0$; the inputs for NAND gate must be let us see all possible cases for $\text{chipselect} = 0$ condition

A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
0	0	0	0	0	0	X	X
0	0	1	1	0	0	X	X
0	1	0	1	0	0	X	X
0	1	1	0	0	0	X	X
1	0	0	1	0	0	X	X
1	0	1	0	0	0	X	X
0	0	0	0	1	1	X	X
0	0	1	1	1	1	X	X
0	1	0	1	0	0	X	X
0	1	1	0	0	0	X	X
1	0	0	1	0	0	X	X
1	0	0	0	0	0	X	X

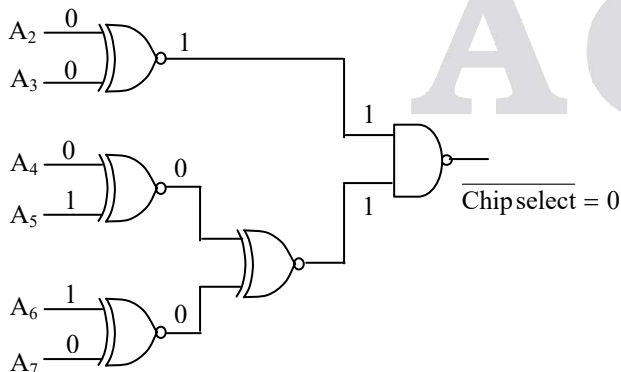
$X \rightarrow 60H (A_1 A_0 = 00)$

$X \rightarrow 63H (A_1 A_0 = 11)$

The only option that suits here is option(a)

A₀ & A₁ are used for line selection

A₂ to A₇ are used for chip selection



\therefore Address space is 60H to 63H

A₀ to A₁₁ are used for line selection

A₁₂ to A₁₅ are used for chip selection

A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁ - - - - - A ₀			
1	1	1	0	0	-	-	0 =E000H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E001H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E002H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E003H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E004H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E005H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E006H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E007H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E008H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E009H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E00AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E00BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E00CH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E00DH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E00EH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E00FH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E010H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E011H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E012H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E013H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E014H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E015H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E016H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E017H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E018H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E019H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E01AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E01BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E01CH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E01DH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E01EH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E01FH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E020H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E021H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E022H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E023H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E024H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E025H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E026H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E027H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E028H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E029H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E02AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E02BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E02CH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E02DH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E02EH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E02FH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E030H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E031H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E032H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E033H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E034H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E035H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E036H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E037H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E038H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E039H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E03AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E03BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E03CH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E03DH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E03EH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E03FH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E040H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E041H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E042H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E043H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E044H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E045H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E046H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E047H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E048H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E049H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E04AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E04BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E04CH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E04DH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E04EH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E04FH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E050H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E051H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E052H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E053H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E054H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E055H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E056H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E057H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E058H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E059H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E05AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E05BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E05CH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E05DH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E05EH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E05FH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E060H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E061H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E062H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E063H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E064H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E065H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E066H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E067H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E068H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	1	-	-	=E069H
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E06AH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0	0	-	-	=E06BH
⋮	⋮	⋮	⋮	⋮			⋮
1	1	1	0				



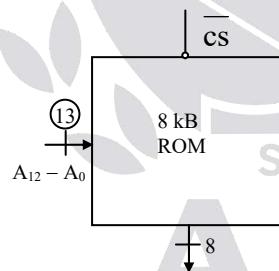
05. Ans: (d)

Sol:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9 - - - - A_0	
0	0	0	0	1	0	0 - - - - 0	=0800H
			⋮			⋮	⋮
0	0	0	0	1	0	1 - - - - 1	=0BFFH
0	0	0	1	1	0	0 - - - - 0	=1800H
			⋮			⋮	⋮
0	0	0	1	1	0	1 - - - - 1	=1BFFH
0	0	1	0	1	0	0 - - - - 0	=2800H
			⋮			⋮	⋮
0	0	1	0	1	0	1 - - - - 1	=2BFFH
0	0	1	1	1	0	0 - - - - 0	=3800H
			⋮			⋮	⋮
0	0	1	1	1	0	1 - - - - 1	=3BFFH

06. Ans: (a)

Sol: Address Range given is



	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1000H →	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2FFFH →	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1

To provide \overline{CS} as low, The condition is

$A_{15} = A_{14} = 0$ and $A_{13} A_{12} = 01$ (or) (10)

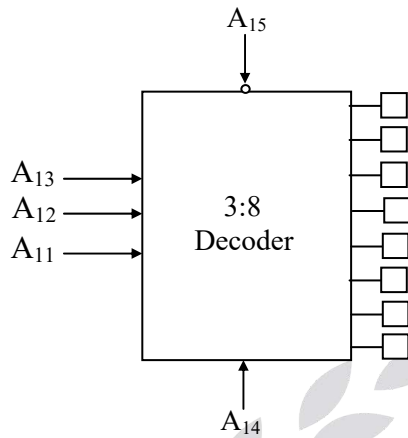
i.e $A_{15} = A_{14} = 0$ and $A_{13} A_{12}$ shouldn't be 00, 11.

Thus it is $A_{15} + A_{14} + [A_{13}A_{12} + \overline{A_{13}}\overline{A_{12}}]$



07. Ans: (a)

Sol:



A_{15}, A_{14} are used for chip selection

A_{13}, A_{12}, A_{11} are used for input of decoder

A_{15} A_{14}	A_{13} A_{12} A_{11}	A_{10} ----- A_0
Enable of decoder	Input of decoder	Address of chip

Size of each memory block = $2^{11} = 2K$

Instruction set of 8085 & Programming with 8085

01. Ans: (c)

Sol:

6010H : LXI H, 8A79H ; (HL) = 8A79H
 6013H : MOV A, L ; (A) ← (L) = 79
 6014H : ADD H ; (A) = 0111 1001
 +
 ; (H) = 1000 1010
 ; (A) = 0000 0011
 CY = 1, AC = 1
 6015H : DAA ; 66 Added to (A)
 since CY=1 &
 AC=1
 ; (A) = 69H
 6016H : MOV H, A ; (H) ← (A) = 69H
 6017H : PCHL ; (PC) ← (HL) = 6979H

02. Ans: (c)

Sol: 0100H : LXI SP, 00FFH ; (SP) = 00FFH
 0103H : LXI H, 0107H ; (HL) = 0107H
 0106H : MVI A, 20H ; (A) = 20H
 0108H : SUB M ; (A) ← (A) - (0107)
 ; (0107) = 20H
 ; (A) = 00H

The contents of Accumulator is 00H

03. Ans: (c)

Sol: SUB1 : MVI A, 00H A ← 00H
 CALL SUB2 → program will shifted to
 SUB 2 address location
 A

SUB 2 : INR A →

01H

RET → returned to the main program

∴ The contents of Accumulator after execution of the above SUB2 is 02H

04. Ans: (c)

Sol: The loop will be executed until the value in register equals to zero, then,

Execution time

$$= 9(7T + 4T + 4T + 10T) + (7T + 4T + 4T + 7T) + 7T$$

$$= 254T$$

05. Ans: (d)

Sol: H=255 : L = 255, 254, 253, ----0

H=254 : L = 0, 255, 254, -----0

H=1 : L = 0, 255, 254, 253, ---0

H=0 : —

→ In first iteration (with H=255), the value in L is decremented from 255 to 0 i.e., 255 times

→ In further remaining 254 iterations, the value in L is decremented from 0 to 0 i.e., 256 times

∴ 'DCRL' instruction gets executed for

$$\Rightarrow [255 + (254 \times 256)]$$

$$\Rightarrow 65279 \text{ times}$$

06. Ans: (a)

Sol: "STA 1234H" is a 3-Byte Instruction and it requires 4 Machine cycles (Opcode fetch, Operand1 Read, Operand2 Read, Memory write). The Higher order Address (A₁₅ – A₈) sent in 4 machine cycles is as follows

Given "STA 1234" is stored at 1FFE H



i.e., Address Instruction

1FFE, 1FFF, 2000 : STA 1234H

Machine cycle	Address (A ₁₅ -A ₀)	Higher order address (A ₁₅ -A ₈)
1. Opcode fetch	1FFE _H	1F _H
2. Operand1 Read	1FFF _H	1F _H
3. Operand2 Read	2000 _H	20 _H
4. Memory Write	1234 _H	12 _H

i.e. Higher order Address sent on A₁₅-A₈ for 4 Machine Cycles are 1F_H, 1F_H, 20_H, 12_H.

07. Ans: (d)

Sol: The operation SBI BE_H indicates A-BE → A where A indicates accumulator. Thus the result of the subtraction operation is stored in the accumulator and the contents of accumulator are changed.

08. Ans: (c)

Sol: If the content in register B is to be multiplied with the content in register C, the contents of register B is added to the accumulator (initial value of accumulator is 0) for C times.

