01. Ans: (d) 
Sol: 
\[135x + 144x = 323x\]
\[(1 \times x^2 + 3 \times x^1 + 5 \times x^0) + (1 \times x^2 + 4 \times x^1 + 4 \times x^0) = 3x^2 + 2x^1 + 3x^0\]
\[\Rightarrow x^2 + 3x + 5 + x^2 + 4x + 4 = 3x^2 + 2x + 3\]
\[x^2 - 5x - 6 = 0\]
\[(x-6)(x+1) = 0\] (Base cannot be negative)
Hence, \(x = 6\).

02. Ans: (a) 
Sol: 
8-bit representation of \(+127_{10}\):
\[+127_{10} = 01111111_{(2)}\]
1’s complement representation of \(-127 = 10000000_{(2)}\).
2’s complement representation of \(-127 = 10000001_{(2)}\).
No. of 1’s in 2’s complement of \(-127 = m = 2\)
No. of 1’s in 1’s complement of \(-127 = n = 1\)
\[\therefore m:n = 2:1\]

03. Ans: (c) 
Sol: 
In 2’s complement representation the sign bit can be extended towards left any number of times without changing the value. In given number the sign bit is ‘X3’, hence it can be extended left any number of times.

04. Ans: (c) 
Sol: 
Binary representation of \((+539)_{10}\):
\[\begin{array}{c}
2539 \\
2269 \ -1 \\
2134 \ -1 \\
267 \ -0 \\
233 \ -1 \\
216 \ -1 \\
28 \ -0 \\
24 \ -0 \\
2 \ -0 \\
1 \ -0
\end{array}\]
\[\text{2'S complement} \rightarrow 11011110011_{(2)}\]
\[\text{Hexadecimal equivalent} \rightarrow (DE5)_{16}\]

05. Ans: 5 
Sol: 
Symbols used in this equation are 0, 1, 2, 3
Hence base or radix can be 4 or higher
\[3x^2 + 1x + 2x^0 = (2x + 0)(x + 3x^0 + x^{-1})\]
\[3x^2 + x + 2 = (2x)(x + 3 + \frac{1}{x})\]
\[3x^2 + x + 2 = 2x^2 + 6x + 2\]
\[x^2 - 5x = 0\]
\[x(x - 5) = 0\]
x = 0 or x = 5
x must be x > 3, So x = 5
06. **Ans:** 3

**Sol:**
\[ 123_5 = x8y \]
\[ 1 \times 5^2 + 2 \times 5^1 + 3 \times 5^0 = x \cdot y^1 + 8 \cdot y^0 \]
\[ 25 + 10 + 3 = xy + 8 \]
\[ \therefore xy = 30 \]

Possible solutions:

i. \( x = 1, y = 30 \)
ii. \( x = 2, y = 15 \)
iii. \( x = 3, y = 10 \)
\[ \therefore 3 \text{ possible solutions exist.} \]

07. **Ans:** 1

**Sol:**

The range (or) distinct values

For 2’s complement \( \Rightarrow -(2^{n-1}) \text{ to } +(2^{n-1}-1) \)

For sign magnitude
\[ \Rightarrow -(2^{n-1}-1) \text{ to } +(2^{n-1}-1) \]

Let \( n = 2 \) \( \Rightarrow \) in 2’s complement
\[ - (2^{2-1}) \text{ to } +(2^{2-1}-1) \]
\[ -2 \text{ to } +1 \Rightarrow -2, -1, 0, +1 \Rightarrow X = 4 \]
\[ n = 2 \text{ in sign magnitude } \Rightarrow -1 \text{ to } +1 \Rightarrow Y = 3 \]
\[ X - Y = 1 \]
01. Ans: (c)
Sol: Given 2’s complement numbers of sign bits are x & y. z is the sign bit obtained by adding above two numbers. \( \therefore \) Overflow is indicated by \( \overline{X} \) = \( \overline{x}y z + x y z \)

Examples
1. A = +7 0111
   B = +7 0111
   14 1110 \( \Rightarrow \overline{x}y z \)
2. A = +7 0111
   B = +5 0101
   12 1100 \( \Rightarrow \overline{x}y z \)
3. A = –7 1001
   B = –7 1001
   –14 10010 \( \Rightarrow xy \overline{z} \)
4. A = –7 1001
   B = –5 1011
   –12 10100 \( \Rightarrow xy \overline{z} \)

02. Ans: (b)
Sol: Truth table of XOR

\[
\begin{array}{ccc}
A & B & o/p \\
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

Stage 1:
Given one i/p = 1 Always.

\[
\begin{array}{ccc}
1 & X & o/p \\
\hline
1 & 0 & 1 \quad = X \\
1 & 1 & 0 \quad = X \\
\end{array}
\]

For First XOR gate o/p = \( X \)

Stage 2:

\[
\begin{array}{ccc}
X & X & o/p \\
\hline
0 & 1 & 1 \\
1 & 0 & 1 \\
\end{array}
\]

For second XOR gate o/p = 1.
Similarly for third XOR gate o/p = \( \overline{X} \) & for fourth o/p = 1
For Even number of XOR gates o/p = 1
For 20 XOR gates cascaded o/p = 1.

03. Ans: (b)
Sol:

\[
\begin{array}{cccc}
\text{w,x} & \text{y,z} & \text{w,x} & \text{y,z} \\
\hline
1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

04. Ans: (c)
Sol:

\[
f_1 \quad f_2 \\
\text{f_3} \\
x = f_1 f_2 \\
f_4 = f_1 \cdot f_2 + f_3
\]

05. Ans: (d)
Sol:

\[
\begin{array}{ccc}
P & Q & B \\
\end{array}
\]
06. Ans: (c)
Sol:  
\[ x_1 \oplus x_3 = x_1 x_3 + x_1 x_3 = y \]
\[ x_2 \oplus x_4 = x_2 x_4 + x_2 x_4 = z \]
\[ (x_1 \oplus x_3) \oplus (x_2 \oplus x_4) = y \oplus z = 0, \text{ when } y = z \]
\[ \therefore \text{ option (c) is true} \]
For all cases option A, B, D not satisfy.

07. Ans: (b)
Sol:  
\[ M(a,b,c) = ab + bc + ca \]
\[ M(a, b, c) = \overline{bc} + \overline{a}b + \overline{a}c \]
\[ M(a, b, \overline{c}) = ab + b\overline{c} + \overline{a}c \]
\[ M( M(a, b, c), M(a, b, \overline{c}), c) \]
\[ = (\overline{bc} + \overline{a}b + \overline{a}c)(ab + bc + ac) \]
\[ + (ab + bc + ac)c + (\overline{bc} + \overline{a}b + \overline{a}c)c \]
\[ = (\overline{bc} + \overline{a}b + \overline{a}c)(ab + bc + ac) \]
\[ + (\overline{bc} + \overline{a}b + \overline{a}c)c + abc \]
\[ = \overline{ab}c + \overline{abc} + abc + \overline{abc} \]
\[ = \overline{c}[\overline{ab} + ab] + c[ab + \overline{ab}] \]

08. Ans: 40
Sol:  
\[ Z = \sum m(1, 2, 4, 7) \]
\[ \therefore M(x, y, z) = a \oplus b \oplus c \]
Where \( x = M(a, b, c), y = M(a, b, \overline{c}), z = c \)

09. Ans: (c)
Sol:  
Logic gates \( \overline{X} + Y = \overline{XY} = \overline{XY_1} \)
Where \( Y_1 = \overline{Y} \)
It is a NAND gate and thus the gate is ‘Universal gate’.
Chapter 3

K - Maps

01. Ans: (b)
Sol:
\[ f = \overline{x}z + x\overline{z} \]

02. Ans: (b)
Sol:
\[ f = \overline{b}\overline{d} + \overline{b}\overline{c} \]

03.
Sol:

04. Ans: (a)
Sol: For n-variable Boolean expression,
Maximum number of minterms = \(2^n\)
Maximum number of implicants = \(2^n\)
Maximum number of prime implicants = \(\frac{2^n - 1}{2}\)

05. Ans: (c)
Sol:
\[ F(A, B, C) = \overline{A}\overline{C} + BC \]

06. Ans: 1
Sol: After minimization = \(\overline{A} + \overline{B} + \overline{C} + D\)
= ABCD
\[ \therefore \text{only one minterm.} \]
07. Ans: 3
Sol: \( \overline{w} \overline{z} + \overline{w} x \overline{y} + \overline{x} \overline{y} \overline{z} \)
01. Ans: (d)
Sol: Let the output of first MUX is “F₁”
\[ F₁ = A₁₀ + A₁₁ \]
Where A is selection line, I₀, I₁ = MUX Inputs
\[ F₁ = \overline{S}_1 \cdot W + S_1 \cdot \overline{W} = S₁ \oplus W \]
Output of second MUX is
\[ F = \overline{A} \cdot I₀ + A \cdot I₁ \]
\[ F = \overline{S}_2 \cdot F₁ + S_2 \cdot \overline{F₁} \]
\[ F = S₂ \oplus F₁ \]
But \( F₁ = S₁ \oplus W \)
\[ F = S₂ \oplus S₁ \oplus W \]
i.e., \( F = W \oplus S₁ \oplus S₂ \)

02. Ans: 50
Sol:
Initially all the output values are ‘0’, at \( t = 0 \), the inputs to the 4-bit adder are changed to \( X₃X₂X₁X₀ = 1100 \), \( Y₃Y₂Y₁Y₀ = 0100 \)
- - - - - - - indicates critical path delay to get the output
Total time taken = $\Delta t_1 + \Delta t_2 = 50$ ns
i.e. critical time (or) maximum time is taken for $Z_4$ to get final output as ‘1’

Total time taken = $\Delta t_1 + \Delta t_2 = 50$ ns
i.e. critical time (or) maximum time is taken for $Z_4$ to get final output as ‘1’
03. Ans: (a)

<table>
<thead>
<tr>
<th>K</th>
<th>C₀</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A+B (addition)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>A+B+1 (addition with carry)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A+⁻B (1’s complement addition)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A+⁻B+1 (2’s complement subtraction)</td>
</tr>
</tbody>
</table>

04. Ans: (d)
Sol: It is expansion of 2:4 decoders to 1:8 demultiplexer A₁, A₀ must be connected to S₁, S₀ i.e.,
R = S₀, S = S₁
Q must be connected to S₂ i.e., Q = S₂
P is serial input must be connected to Dᵢn

05. Ans: 6
Sol: T = 0 → NOR → MUX 1 → MUX 2
2ns 1.5ns 1.5ns
Delay = 2ns + 1.5ns + 1.5ns = 5ns
T = 1 → NOT → MUX 1→NOR→ MUX 2
1ns 1.5ns 2ns 1.5ns
Delay = 1ns + 1.5ns + 2ns + 1.5ns = 6ns
Hence, the maximum delay of the circuit is 6ns

06. Ans: –1
Sol: When all bits in ‘B’ register is ‘1’, then only it gives highest delay.

∴ ‘–1’ in 8 bit notation of 2’s complement is 1111 1111
Sequential Circuits

01. Ans: (c)
   Sol: Given Clk, X1, X2
   Output of First D-FF is Q1
   Output of Second D-FF is Q2

   As the clear input is given to be synchronous so it waits upto the next clock pulse to clear the counter & hence the counter get's cleared during the 7th clock pulse.
   \[ \therefore \] mod of counter = 7

02. Ans: 4
   Sol: In the given first loop of states, zero has repeated 3 times. So, minimum 4 number of Flip-flops are needed.

03. Ans: 7
   Sol: The counter is cleared when
   \[ Q_DQ_CQ_BQ_A = 0110 \]

   The counter is cleared when
   \[ Q_DQ_CQ_BQ_A = 0110 \]

04. Ans: (b)
   Sol: The given circuit is a mod 4 ripple down counter. Q1 is coming to 1 after the delay of 2Δt.

<table>
<thead>
<tr>
<th>CLK</th>
<th>Q1</th>
<th>Q0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

05. Ans: (c)
   Sol: Assume n = 2

   Outputs of counter is connected to inputs of decoder

<table>
<thead>
<tr>
<th>Counter outputs</th>
<th>Decoder inputs</th>
<th>Decoder outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_D Q_C Q_B Q_A</td>
<td>a b</td>
<td>d1 d2 d3 d4</td>
</tr>
<tr>
<td>{0 0 0 0}</td>
<td>0 0</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>0 1</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>1 0</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>1 1</td>
<td>1 0 0 0</td>
</tr>
</tbody>
</table>

   The overall circuit acts as 4-bit ring counter
   \[ n = 2 \]
   \[ \therefore k = 2^2 = 4, k-bit ring counter \]
06. Ans: (b)  
Sol:

<table>
<thead>
<tr>
<th>CLK</th>
<th>Serial in= B ⊕ C ⊕ D</th>
<th>A B C D</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1 0 1 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1 1 0 1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0 0 1 1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1 0 0 0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1 0 1 0</td>
</tr>
</tbody>
</table>

: After 7 clock pulses content of shift register become 1010 again

07. Ans: (b)  
Sol:

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Qn</th>
<th>T = (J+Qn) (K+Qn)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.1 = 0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.0 = 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0.1 = 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1.1 = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1.1 = 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.0 = 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1.1 = 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.1 = 0</td>
</tr>
</tbody>
</table>

\[ T = J \bar{Q}_n + KQ_n = (J+Q_n) (K+\bar{Q}_n) \]

08. Ans: 1.5  
Sol:

<table>
<thead>
<tr>
<th>C/lk</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q5</th>
<th>Y = Q3 + Q5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The waveform at OR gate output, Y is [A = +5V]

\[ A \]

Average power

\[
    P = \frac{V^2}{R} = \frac{1}{R} \left[ \frac{1}{T_1} \int_{t_0}^{t_1} y^2(t) \, dt \right] = \frac{1}{RT_1} \left[ \int_{t_0}^{2T} A^2 \, dt + \int_{2T}^{5T} A^2 \, dt \right]
\]

\[
    = \frac{A^2}{RT_1} \left[ (2T - T) + (5T - 3T) \right] = \frac{A^2 \cdot 3T}{R(5T)} = \frac{5^2 \cdot 3}{10 \times 5} = 1.5 \text{ mw}
\]
09. Ans: (b)
Sol:

<table>
<thead>
<tr>
<th>Present State</th>
<th>X = 0</th>
<th>X = 1</th>
<th>X = 0</th>
<th>X = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>A</td>
<td>E</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>C</td>
<td>A</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>D</td>
<td>A</td>
<td>B</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>E</td>
<td>A</td>
<td>C</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Reducing state table

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
</tr>
</thead>
<tbody>
<tr>
<td>X = 0</td>
<td>X = 1</td>
</tr>
<tr>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>C</td>
<td>C</td>
</tr>
<tr>
<td>D</td>
<td>D</td>
</tr>
</tbody>
</table>

Finally reduced state table is

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
</tr>
</thead>
<tbody>
<tr>
<td>X = 0</td>
<td>X = 1</td>
</tr>
<tr>
<td>A</td>
<td>D</td>
</tr>
<tr>
<td>B</td>
<td>A</td>
</tr>
<tr>
<td>D</td>
<td>B</td>
</tr>
</tbody>
</table>

: 3 states are present in the reduced state table

10. Ans: (c)
Sol: State table for the given state diagram

<table>
<thead>
<tr>
<th>State</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S₀</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>S₀</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>S₁</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>S₁</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Output is 1’s complement of input.

11. Ans: (c)
Sol: In state (C), when XYZ = 111, then Ambiguity occurs
Because, from state (C)
⇒ When X = 1, Z = 1
⇒ N.S is (A)
When Y = 1, Z = 1 ⇒ N.S is (B)
01. Ans: (b)
Sol: \( V_{OH}(\text{min}) \):
(High level output voltage)
The minimum voltage level at a Logic circuit output in the logic ‘1’ state under defined load conditions.

\( V_{OL}(\text{max}) \):
(Low level output voltage)
The maximum voltage level at a logic circuit output in the Logical ‘0’ state under defined load conditions.

\( V_{IL}(\text{max}) \):
(Low level input voltage)
The maximum voltage level required for a logic ‘0’ at an input. Any voltage above this level will not be accepted as a Low by the Logic circuit.

\( V_{IH}(\text{min}) \):
(High level input voltage)
The minimum voltage level required for logic ‘1’ at an input. Any voltage below this level will not be accepted as a HIGH by the Logic circuit.

02. Ans: (b)
Sol: Fan out is minimum in DTL
(High Fan-out = CMOS)
Power consumption is minimum in CMOS.
Propagation delay is minimum in ECL
(fastest = ECL)

03. Ans: (b)
Sol: When \( V_i = 2.5V \),
\( Q_1 \) is in reverse active region
\( Q_2 \) is in saturation region
\( Q_3 \) is in saturation region
\( Q_4 \) is in cut-off region

04. Ans: (d)
Sol: The given circuit can be redrawn as below:

05. Ans: (b)
Sol: As per the description of the question, when the transistor \( Q_1 \) and diode both are OFF then only output \( z = 1 \).

<table>
<thead>
<tr>
<th>( X )</th>
<th>( Y )</th>
<th>( Z )</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>( Q_1 ) is OFF, Diode is ON</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>( Q_1 ) is OFF, Diode is OFF</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>( Q_1 ) is ON, Diode is OFF</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( Q_1 ) is ON, Diode is OFF</td>
</tr>
</tbody>
</table>

Hence \( Z = \overline{XY} \)
Chapter 7

Semiconductor Memories

01. Ans: (b)
Sol: Square of a 4 - bit number can be at most 8 - bit number.
\{(i.e \((1111)_2 = (15)_{10}\)
\)[\((15)_{10}\)^2 = (225)_{10}\].
Therefore ROM requires 8 data lines.
Data is with size of 4 bits
ROM must require 4 address lines and 8 data lines
\(ROM = 2^n \times m\)
\(n = \text{inputs (address lines)},\)
\(m = \text{output lines}\)
\(n = 4, m = 8.\)

02. Ans: (a)
Sol: ROM is used to design a combinational circuit. The number of address lines of the ROM is equal to the number of input variables in the truth table.
ROM is represented as \(2^n \times m\) where \(2^n\) inputs and \(m\) output lines.
[Where \(n = \text{address bits}\]

03. Ans: (b)
Sol:
<table>
<thead>
<tr>
<th>8</th>
<th>4</th>
<th>2</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>X2</td>
<td>X3</td>
<td>X4</td>
<td>Y1</td>
<td>Y2</td>
<td>Y3</td>
<td>Y4</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The outputs are in 2 4 2 1 BCD number

04. Ans: (c)
Sol:

At the rising edge of the First clock pulse the content of location \((0110)_2 = 6 \Rightarrow 1010\) appears on the data bus, at the rising of the second clock pulse the content of location \((1010)_2 = 10_2 \Rightarrow 1000\) appears on the data bus.

05. Ans: (b)
Sol: 1–bit SRAM memory cell is

In 2 Inverters, output of the 1st Inverter is connected to Gate Input of 2nd Inverter and vice versa.
A/D & D/A Converters

01. Ans: (b)
Sol:

<table>
<thead>
<tr>
<th>CLK</th>
<th>Counter Q2 Q1 Q0</th>
<th>Decoder D3 D2 D1 D0</th>
<th>V0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0 0 0</td>
<td>0 0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0 0 1</td>
<td>0 0 0 1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0 1 0</td>
<td>0 0 1 0</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>0 1 1</td>
<td>0 0 1 1</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>1 0 0</td>
<td>1 0 0 0</td>
<td>8</td>
</tr>
<tr>
<td>6</td>
<td>1 0 1</td>
<td>1 0 0 1</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>1 1 0</td>
<td>1 0 1 0</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>1 1 1</td>
<td>1 0 1 1</td>
<td>11</td>
</tr>
</tbody>
</table>

V0 = -Ii R = \(-\frac{5I}{16}\) \times 10k\,\Omega
= \(-\frac{5\times10^{-3}\times10^{10}}{16}\) = -3.125V

02. Ans: (b)
Sol:

R_{equ} = (((((2R||2R)+R)||2R)+R)||2R)+R)||2R)
R_{equ} = R = 10k\,\Omega

R = \frac{10V}{10k} = 1mA.

Current division at \frac{1}{16}
= \frac{1\times10^{-3}}{16} = 62.5\,\mu A

03. Ans: (c)
Sol: Net current at inverting terminal,

I_i = \frac{1}{4} + \frac{1}{16} = \frac{5I}{16}

04. Ans: (d)
Sol: Given that \(V_{DAC} = \sum_{n=0}^{3} 2^n b_n\) Volts
\(V_{DAC} = 2^{-1}b_0 + 2^0 b_1 + 2^1 b_2 + 2^2 b_3\)
\Rightarrow V_{DAC} = 0.5b_0 + b_1 + 2b_2 + 4b_3

Initially counter is in 0000 state

<table>
<thead>
<tr>
<th>Up counter o/p b_3 b_2 b_1 b_0</th>
<th>V_{DAC}(V)</th>
<th>o/p of comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>1.5</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>2.5</td>
<td>1</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>3.5</td>
<td>1</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>4.5</td>
<td>1</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>5.5</td>
<td>1</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>6.5</td>
<td>0</td>
</tr>
</tbody>
</table>

When \(V_{DAC} = 6.5\,V\), the o/p of comparator is ‘0’. At this instant, the clock pulses to the counter are stopped and the counter remains in 1101 state.

:. The stable reading of the LED display is 13.
05. Ans: (b)  
Sol: The magnitude of error between $V_{DAC}$ & $V_{in}$ at steady state is $|V_{DAC} - V_{in}| = |6.5 - 6.2| = 0.3 \, V$.

06. Ans: (a)  
Sol: In Dual slope

$$\text{ADC} \Rightarrow V_{in} T_1 = V_R T_2$$

$$\Rightarrow V_{in} = \frac{V_R T_2}{T_1} = \frac{100 \, mV \times 370.2 \, ms}{300 \, ms} = 123.4$$

DVM indicates $= 123.4$

07. Ans: (d)  
Sol: Ex: $f_{in} = 1 \, kHz \rightarrow f_s = 2 \, kHz$

$f_{in} = 25 \, kHz \leftrightarrow f_s = 50 \, kHz$

1. Max conversion time $= 2^{N+1}T = 2^{11.1} \, \mu s = 2048 \, \mu s$

2. Sampling period $= T_s \geq$ maximum conversion time $T_s \geq 2048 \, \mu s$

3. Sampling rate $f_s = \frac{1}{T_s} \leq \frac{1}{2048 \times 10^{-6}} = 488 \, Hz \leq f_s \leq 500 \, Hz$

4. $f_{in} = \frac{f_s}{2} = 250 \, Hz$
Chapter

9

Architecture, Pin Details of 8085 & Interfacing with 8085

01. Ans: (a)
Sol: chip select is an active low signal for chipselect = 0; the inputs for NAND gate must be let us see all possible cases for chipselect = 0 condition

<table>
<thead>
<tr>
<th>A7</th>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

The only option that suits here is option(a)

A0 & A1 are used for line selection
A2 to A7 are used for chip selection

02. Ans: (d)
Sol:
- Both the chips have active high chip select inputs.
- Chip 1 is selected when A8 = 1, A9 = 0
- Chip 2 is selected when A8 = 0, A9 = 1
- Chips are not selected for combination of 00 & 11 of A8 & A9
- Upon observing A8 & A9 of given address Ranges, F800 to F9FF is not represented

03. Ans: (d)
Sol: The I/O device is interfaced using “Memory Mapped I/O” technique.
The address of the Input device is

```
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
1 1 1 1 1 0 0 0 1 1 1 1 1 0 0 =F8F8H
```

The Instruction for correct data transfer is

```
LDA F8F8H
```

04. Ans: (b)
Sol:
- Out put 2 of 3×8 Decoder is used for selecting the output port. ∴ Select code is 010
- 5000H
- This mapping is memory mapped I/O
05. **Ans: (d)**

**Sol:**

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - - - - 0</td>
</tr>
</tbody>
</table>

=0800H

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - - - - 1</td>
</tr>
</tbody>
</table>

=0BFFH

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - - - - 1</td>
</tr>
</tbody>
</table>

=1BFFH

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - - - - 0</td>
</tr>
</tbody>
</table>

=2800H

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - - - - 1</td>
</tr>
</tbody>
</table>

=2BFFH

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - - - - 0</td>
</tr>
</tbody>
</table>

=3800H

<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A₀ - - - - A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 - - - - 1</td>
</tr>
</tbody>
</table>

=3BFFH

06. **Ans: (a)**

**Sol:** Address Range given is

```
<table>
<thead>
<tr>
<th>A₁₅</th>
<th>A₁₄</th>
<th>A₁₃</th>
<th>A₁₂</th>
<th>A₁₁</th>
<th>A₁₀</th>
<th>A₉</th>
<th>A₈</th>
<th>A₇</th>
<th>A₆</th>
<th>A₅</th>
<th>A₄</th>
<th>A₃</th>
<th>A₂</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
```

To provide \( \bar{cs} \) as low, The condition is

\( A₁₅ = A₁₄ = 0 \) and \( A₁₃ \ A₁₂ = 01 \) (or) \( 10 \)

i.e \( A₁₅ = A₁₄ = 0 \) and \( A₁₃ \ A₁₂ \) shouldn’t be \( 00, 11 \).

Thus it is \( A₁₅ + A₁₄ + [A₁₃ \ A₁₂ + A₁₃ \ A₁₂] \)
07. Ans: (a)
Sol:

\[ A_{15}, A_{14} \text{ are used for chip selection} \]
\[ A_{13}, A_{12}, A_{11} \text{ are used for input of decoder} \]

<table>
<thead>
<tr>
<th>A_{15}</th>
<th>A_{14}</th>
<th>A_{13}</th>
<th>A_{12}</th>
<th>A_{11}</th>
<th>A_{10}</th>
<th>\ldots</th>
<th>A_0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable of decoder</td>
<td>Input of decoder</td>
<td>Address of chip</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Size of each memory block = \(2^{11} = 2K\)
Chapter 10

Instruction set of 8085 & Programming with 8085

01. Ans: (c)
Sol:
6010H : LXI H, 8A79H ; (HL) = 8A79H
6013H : MOV A, L ; (A) ← (L) = 79
6014H : ADD H ; (A) = 0111 1001 +
        ; (H) = 1000 1010
        ; (A) = 0000 0011
        CY = 1, AC = 1
6015H : DAA ; 66 Added to (A)
since CY=1 & AC=1
        ; (A) = 69H
6016H : MOV H, A ; (H) ← (A) = 69H
6017H : PCHL ; (PC) ← (HL) = 6979H

RET → returned to the main program
∴ The contents of Accumulator after execution of the above SUB2 is 02H

02. Ans: (c)
Sol:
0100H : LXI SP, 00FFH ; (SP) = 00FFH
0103H : LXI H, 0107H ; (HL) = 0107H
0106H : MVI A, 20H ; (A) = 20H
0108H : SUB M ; (A) ← (A) - (0107)
        ; (0107) = 20H
        ; (A) = 00H
The contents of Accumulator is 00H

03. Ans: (c)
Sol:
SUB1 : MVI A, 00H A ← 00H
CALL SUB2 → program will shifted to
SUB 2 address location
SUB 2 : INR A → A

04. Ans: (c)
Sol: The loop will be executed until the value in register equals to zero, then,

Execution time
= 9(7T + 4T + 4T + 10T) + (7T + 4T + 4T + 7T) + 7T
= 254T

05. Ans: (d)
Sol:
H=255 : L = 255, 254, 253, ----0
H=254 : L = 0, 255, 254, -------0
   H=1 : L = 0, 255, 254, 253, ---0
   H=0 : ---
→ In first iteration (with H=255), the value in L is decremented from 255 to 0 i.e., 255 times
→ In further remaining 254 iterations, the value in L is decremented from 0 to 0 i.e., 256 times
∴ 'DCRL' instruction gets executed for
⇒ [255 + (254 × 256)]
⇒ 65279 times

06. Ans: (a)
Sol: “STA 1234H” is a 3-Byte Instruction and it requires 4 Machine cycles (Opcode fetch, Operand1 Read, Operand2 Read, Memory write). The Higher order Address (A15–A8) sent in 4 machine cycles is as follows

Given “STA 1234” is stored at 1FFEH
i.e., Address Instruction

1FFE, 1FFF, 2000 : STA 1234H

<table>
<thead>
<tr>
<th>Machine cycle</th>
<th>Address (A15-A0)</th>
<th>Higher order address (A15-A8)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Opcode fetch</td>
<td>1FFEH</td>
<td>1FH</td>
</tr>
<tr>
<td>2. Operand1 Read</td>
<td>1FFFH</td>
<td>1FH</td>
</tr>
<tr>
<td>3. Operand2 Read</td>
<td>2000H</td>
<td>20H</td>
</tr>
<tr>
<td>4. Memory Write</td>
<td>1234H</td>
<td>12H</td>
</tr>
</tbody>
</table>

i.e. Higher order Address sent on A15-A8 for 4 Machine Cycles are 1FH, 1FH, 20H, 12H.

07. Ans: (d)

Sol: The operation SBI BEH indicates A-BE → A where A indicates accumulator
Thus the result of the subtraction operation is stored in the accumulator and the contents of accumulator are changed.

08. Ans: (c)

Sol: If the content in register B is to be multiplied with the content in register C, the contents of register B is added to the accumulator (initial value of accumulator is 0) for C times.