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ESE- 2018 (Prelims) - Offline Test Series-Test-1

ELECTRICAL ENGINEERING

SUBJECT: ANALOG AND DIGITAL ELECTRONICS + BASIC ELECTRONICS ENGINEERING – SOLUTIONS

01. Ans: (c)

Sol: The given circuit is a wein-bridge oscillator

The condition for sustained oscillations (or) the minimum voltage gain required to maintain the oscillations in a wein-Bridge oscillator is

$$A_V = 1+\frac{R_1}{R_2}+\frac{C_2}{C_1} \text{ ------- (1)}$$ [where R_1 = 2R, R_2 = R, C_1 = C and C_2 = 2C in the given circuit]

$$\Rightarrow 1+\frac{R_f}{R_1}=1+\frac{2R}{R}+\frac{2C}{C}=5 \text{ -------- (2)}$$

$\Rightarrow R_f/R_1 = 4$ ------- (3)

$\therefore R_f = 4R_1$ ------(4)

02. Ans: (c)

Sol: Step (1):

When $V_i = -2V$, $V_A = -12V$

Step (2):

$\because V_A = -12V$, D is OFF $\Rightarrow V_0 = 0V$

03. Ans: (d)

Sol: Step (1): KCL at collector node of Q_1

$$I_{Ref} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$= I_{C_1} + 2I_{B_2}$$

$$= I_{C_2} + \frac{2I_{C_2}}{\beta}$$

$$= I_{C_2}\left[1+\frac{2}{\beta}\right]$$

$$\therefore \frac{I_{Ref}}{I_{C_2}} = \frac{I_{Ref}}{I_0} = 1+\frac{2}{50} = 1.04$$

04. Ans: (b)

Sol: Step (1):

$$f_{L_f} = \frac{f_L}{1+A\beta} = \frac{2kHz}{1+1000\times 0.01} = 181.818Hz$$

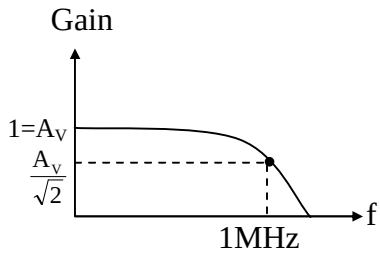
Step (2):

$$f_{H_f} = f_H(1+A\beta)$$

$$= 20\text{kHz} \times (1+1000\times 0.01) = 220\text{kHz}$$

05. Ans: (b)

Sol:



Bandwidth = f_H = 1MHz

At f_H, Gain of the amplifier, $A_V = \frac{1}{\sqrt{2}}$

$$\Rightarrow A_V = \frac{V_0}{V_i} = \frac{1}{\sqrt{2}} V$$

$$V_0 = \frac{V_i}{\sqrt{2}} = \frac{2}{\sqrt{2}} = \sqrt{2}\ V$$

06. Ans: (a)

07. Ans: (b)

08. Ans: (b)

Sol: In negative feedback amplifiers

Voltage gain ↓

Bandwidth ↑

Noise ↓

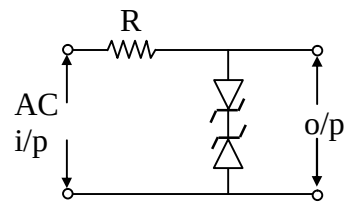
Distortion ↓

Amplitude fluctuations ↓

09. Ans: (a)

10. Ans: (d)

Sol:



11. Ans: (a)

Sol: $V_H = 2V_{sat}\left(\frac{R_2}{R_1+R_2}\right)$

$$= 2\times 10\left(\frac{1}{1+9}\right) = 2\text{V}$$

12. Ans: (c)

Sol: V_0= gain × input voltage

$$= A \times V_m \sin\omega t \ \text{(i.e., } A\times V_m = V_x)$$

$$\frac{dV_0}{dt} = V_x \cos\omega t \times \omega$$

$$SR = \left.\frac{dV_0}{dt}\right|_{max} = V_x 2\pi f$$

$$\Rightarrow 100\times 10^6 = V_x \times 2\pi \times 20\times 10^6$$

$$V_x = \frac{100}{40\pi} = \frac{5}{2\pi} V$$

13. Ans: (c)

Sol: $V_0 = -2(2) = -4\text{V}$

$$I_0 = -\frac{V_0}{2k} + \left(\frac{-V_0}{1k}\right)$$

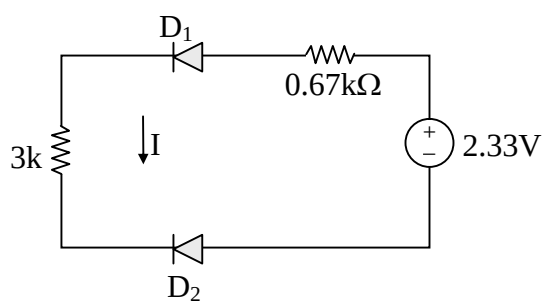
$$= 2\times 10^{-3} + 4\times 10^{-3}$$

$$= 6\ \text{mA}$$

14. Ans: (a)

Sol: both the diodes are OFF

$I = 0$

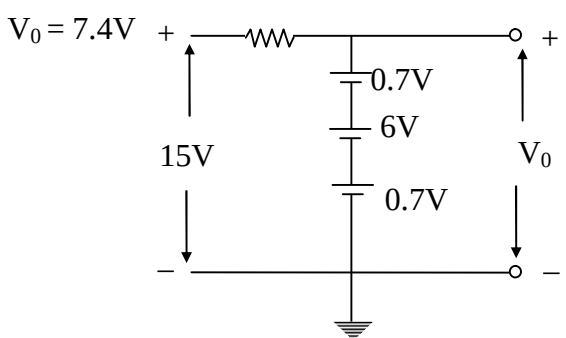


15. Ans: (c)

Sol: $D \rightarrow F\ B$

$Z_1 \rightarrow$ operated in break down region

$Z_2 \rightarrow F\ B$ then



16. Ans: (b)

17. Ans: (d)

Sol: $V_0 = \frac{R_2}{R_1} \times (V_1 - V_2)$

$V_1 - V_2 = -2V$

$V_0 = 5(-2)$

$= -10V$

18. Ans: (a)

Sol: For negative feedback, gain factor is reduces by $(1 + A\beta)$ for shunt-series, R_{in} is decreased by a factor of $(1+A\beta)$, R_0 is increased by a factor of $(1 + A\beta)$

19. Ans: (a)

Sol: Here the base emitter voltage is greater than 0.7 V and the base collector voltage is less than 0.7 V.
Hence base emitter junction is in forward bias and collector-base junction is in reverse bias.
$\therefore$ Transistor is in forward active region

20. Ans: (d)

Sol: Here I_{CBO} doubles for every 10^0 raise in temperature V_{BE} decreases at the rate of 2.5 mV/^{0}C

21. Ans: (d)

Sol: P $\rightarrow$ RC coupled amplifier $\rightarrow$ Audio

Q $\rightarrow$ Differential amplifier $\rightarrow$ DC and audio

R $\rightarrow$ Cascode amplifier $\rightarrow$ Video

S $\rightarrow$ Tuned amplifier $\rightarrow$ Narrow band

22. Ans: (d)

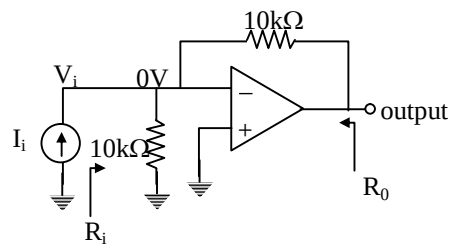
Sol: The oscillation frequency in crystal oscillator is determined by the crystal dimensions. This means that crystal oscillator frequency depends on all of the above parameters i.e. thickness of crystal, angle of cut and physical size of crystal

23. Ans: (a)

Sol: The transistor with comparatively small β is used in power amplifier because to handle large currents base of the transistor is made thicker. Hence β should be small

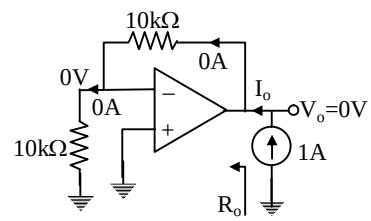
24. Ans: (b)

Sol:



$$\text{Input resistance } (R_i) = \frac{V_i}{I_i} = \frac{0}{0.5m} = 0\Omega$$

For output resistance, input current 0.5mA is open circuited & connected 1A current source at output as show in below figure.



$$\Rightarrow \text{Output resistance } (R_o) = \frac{V_o}{I_o} = \frac{0}{1} = 0\Omega$$

25. Ans (c)

Sol: The Common Emitter current gain – bandwidth product of a transistor (f_T) is defined as the frequency at which Beta of the transistor falls to unity

Unity gain frequency $(f_T) = \dfrac{g_m}{2\pi(C_\pi + C_\mu)}$

26. Ans: (a)

Sol: The bias stability of an Emitter-Bias Amplifier circuit improves by decreasing the value of R_B and increasing the value of R_E.

27. Ans: (d)

Sol: $A_V = -g_m r_{01}$

$$= \frac{-I_{EE}/2}{V_t}\left[\frac{V_A}{I_{EE}/2}\right]$$

$$= \frac{-V_A}{V_t} = \frac{-5}{0.026} = -192.31$$

28. Ans: (d)

Sol: In current series feedback output current is proportional to input voltage. Hence it is Transconductance amplifier.

29. Ans: (a)

Sol: When two pure conductors are added then resistivity increases at all time

30. Ans: (c)

Sol: $\lambda_{max} = \dfrac{1.24}{E_G(eV)}\mu m$

$$= \frac{1.24}{2.5}\mu m = 0.496\ \mu m = 4960\ A^o$$

31. Ans: (a)

Sol: Junction capacitance $\alpha \dfrac{1}{\text{Junction Voltage}}$

Step: $C_j \propto \dfrac{1}{\sqrt{V_S}} \rightarrow \dfrac{1}{2}$

Linear: $C_j \propto \dfrac{1}{\sqrt[3]{V_S}} \rightarrow \dfrac{1}{3}$

Diffused = $C_j \propto \dfrac{1}{\sqrt[2.5]{V_S}} \rightarrow \dfrac{1}{2.5}$

32. Ans: (b)

Sol: Voltage shunt feed back

33. Ans: (b)

Sol: $I_D = I_{Dss}\left(1 - \dfrac{V_{gs}}{V_p}\right)^2$

Transconductance of (g_m) FET is

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{2I_{Dss}}{-Vp}\left(1 - \frac{V_{gs}}{V_p}\right)$$

$$\left[\because \left(1 - \frac{V_{gs}}{V_p}\right)^2 = \frac{I_D}{I_{Dss}}\right]$$

$$g_m = \frac{2}{|v_p|}\sqrt{I_D . I_{Dss}}$$

34. Ans: (d)

Sol: Once an SCR is turned on, it will remain so until the anode current goes below to holding current value.

35. Ans: (d)

Sol: LED is made by a direct band gap material.

$$E_g = \frac{hc}{\lambda}$$

The colour of the light has a particular wavelength λ according to the band gap energy of semiconductor material

36. Ans: (a)

Sol: The auto correlation function of White Noise is a delta function.

$$\delta(t) \xleftrightarrow[\text{Pair}]{\text{FT}} 1$$

$$\text{So } \frac{N_0}{2}\delta(t) \xleftrightarrow[\text{Pair}]{\text{FT}} \frac{N_0}{2}$$

37. Ans: (c)

Sol: $P_c = 1.8$ KW

$$P_{SB} = \frac{P_C \mu^2}{4} = 200\,\text{W}$$

$$\frac{1.8\times10^3 \times \mu^2}{4} = 200\,\text{W}$$

$$\mu^2 = 4/9$$

$$\mu = \sqrt{\frac{4}{9}} = \frac{2}{3} = 0.666$$

$\% \mu = 66.66\%$

38. Ans: (c)

Sol: modulation index of AM

$\mu = k_a A_m$ which is independent of frequency

FM $\beta_f = \frac{k_f A_m}{f_m}$

f_m doubled, β_f is half

PM $\beta_p = k_p A_m$, independent of frequency

39. Ans: (b)

Sol: For entropy of source

$S_1 = \log_2 4 = 2\log_2 2$

=2 bits/symbol

For entropy or source

$S_2 = \log_2 16 = 4\log_2 2$

= 4 bits/symbol

40. Ans: (b)

Sol: If L = 2 $\rightarrow$ Data word length n= 1bit.

Data rate = n f_s b/sec

= f_s bits/sec,

Where f_s is the sampling rate.

If L = 8 $\rightarrow$ n = 3 bits.

Data rate = $3f_s$ bps.

Since (B.W) $\propto$ data rate, B.W requirement gets tripled.

41. Ans: (b)

Sol: The signal is received using the pre-selection stage, i.e. an RF amplifier. It is mixed with local oscillator and IF is generated. It is amplified by the IF amplifier and the amplitude variations are removed by amplitude limiter. Then, it is applied to the FM demodulator. The demodulated signal is amplified by an audio amplifier.

42. Ans: (c)

Sol: Typical Uplink & Downlink frequencies used in satellite communication are

Uplink	**Downlink**
6 GHz	4 GHz
14 GHz	12 GHz
30 GHz	24 GHz

43. Ans: (d)

Sol: Flash memory takes more number of Read/Write cycles

44. Ans: (a)

Sol: In PLA $\Rightarrow$ both "AND" and "OR" programmable

(iii) Represents Fan out

45. Ans: (b)

Sol: $2^N \geq$ (no of digits in sequence) + 1

N: number of flip-flops

$2^N \geq 5 + 1$

$N = 3$

So number of flip-flops = 3

46. Ans: (a)

Sol: Using SOP form

$$Y = \overline{A}\ \overline{B}\ (1) + \overline{A}\ B(1) + A\,\overline{B} + AB(B)$$

$$= \overline{A}\ \overline{B} + \overline{A}\ B + A\ \overline{B} + A\,B$$

$$=1$$

Using POS form

$$Y = (A + B + 1)(A + \overline{B} + 1)(\overline{A} + B + A)(\overline{A} + \overline{B} + B)$$

= (1) (1) (1) (1)

= 1

47. Ans: (b)

Sol: $x \oplus y = \overline{x \odot y}$

$$= \overline{xy + \overline{x}\,\overline{y}}$$

$$= \overline{0 + \overline{x}\,\overline{y}} = \overline{\overline{x}\,\overline{y}} = x + y$$

OR gate

48. Ans: (a)

Sol:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

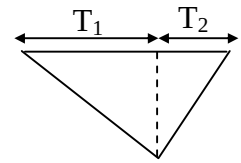
$X = D_4 + D_5 + D_6 + D_7$

$Y = D_2 + D_3 + D_6 + D_7$

$Z = D_1 + D_3 + D_5 + D_7$

49. Ans: (c)

Sol:



$(V_{in}).\ T_1 = (V_{ref}).\ T_2$

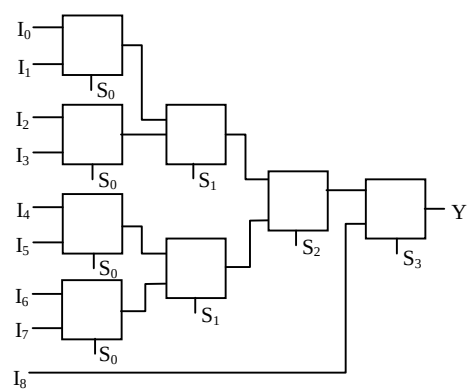
(1) (10×20msec) = (2) T_2

T_2 = 100msec

Total time = $T_1 + T_2$ = 0.3sec

50. Ans: (c)

Sol: Implementation is as shown



51. Ans: (d)

Sol: $X = (P + Q + R)(\overline{P} + Q + \overline{R})$

$= PQ + P\overline{R} + \overline{P}Q + Q + Q\overline{R} + \overline{P}R + QR$

$= Q(1 + P + \overline{P} + \overline{R} + R) + \overline{P}R + \overline{P}R$

$= (P \oplus R) + Q$

52. Ans: (b)

Sol: $\sqrt{3r^2 + r + 1} = r + 4$

$3r^2 + r + 1 = r^2 + 8r + 16$

$2r^2 - 7r - 15 = 0$

$2r^2 - 10r + 3r - 15 = 0$

$2r(r - 5) + 3(r - 5) = 0$

$(r - 5)\ (2r + 3) = 0$

$r = 5$ or -1.5 (invalid)

53. Ans: (b)

Sol: XOR operation gives output HIGH, when odd no. of input variables are HIGH. So, by looking at the truth table. Option 1 and 3 are correct.

AB \ CD	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

54. Ans: (a)

Sol: Cache memory is a very high speed memory that is placed between the CPU and main memory. The cache stocks the copies of the data from frequently used main memory locations

Inter leaving: main memory is divided into two or more sections. The CPU can access alternate sections immediately without waiting for memory to catch up (through wait states)

55. Ans: (c)

Sol: CMOS inverter is formed by the series connection of one n-channel and one p-channel MOS transistor

Whereas transmission gate is formed by the parallel connection of one p-channel and one n-channel MOS transistors

56. Ans: (a)

57. Ans: (b)

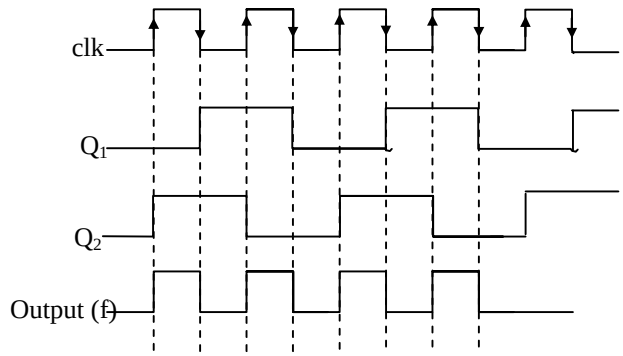
Sol:

Clk pulse	Input	Q_3	Q_2	Q_1
0		0	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	1	1
4	0	0	1	1
5	0	0	0	1
6	0	0	0	0

$\overline{Q_1}$ is fed as input in Johnson counter

58. Ans: (a)

Sol:



Output is same as clk

$\therefore$ The frequency of output is 50MHz

59. Ans: (c)

Sol: $F_1.F_2 = \Sigma m(4,6) + d(1, 2, 3, 7)$

$\downarrow$

(common minterms of F_1,F_2)

$F_1+F_2 = \Sigma m(0, 1, 2, 3, 4, 6) + d(7)$

$(F.F_2) + (F_1+F_2) = \Sigma m(0,1,2,3,4,6)+d(7)$

$d.0 = 0$

$d.d = d$

$1.d = d$

$d + d = d$

$1 + d = 1$

$0 + d = d$

60. Ans: (c)

Sol: the time taken for SIPO is

$T_1 = NT$

The time taken for SISO is

$T_2 = (2N–1)\ T$

$T_2–T_1 = (N–1)\ T$

61. Ans: (c)

Sol: (a),(b) are operations Performed when RESETIN is made low

(c) is performed when RESET out is made high

(d) is performed during DMA data transfer

62. Ans: (d)

Sol:

```
0100   MVI     A, 00H
0102   LXI     H, 0105H
0105   OUT     00H
0106   INR     A
0107   PCHL
0108   HLT
```

$A \leftarrow 00$		
$HL \leftarrow 0105$	$01 \rightarrow [00]$	$02 \rightarrow [00]$
$A \rightarrow [00]$	$A \leftarrow 02$	$A \leftarrow 03$
$A \rightarrow 01$	$PC \leftarrow 0105$	$PC \leftarrow 0105$
$PC \leftarrow 0105$		

Infinite Loop

63. Ans: (a)

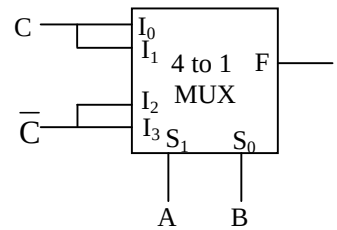
Sol: Given $A + A\overline{B} + A\overline{B}\ C$

$= A\ (1 + \overline{B} + \overline{B}\ C) = A$

No NAND gate is required to implement the expression

64. Ans: (d)

Sol:



$$F = \overline{A}\overline{B}C + \overline{A}\,BC + A\overline{B}\overline{C} + AB\overline{C}$$

$$F = \overline{A}C\left(B + \overline{B}\right) + A\overline{C}\left(B + \overline{B}\right)$$

$$F = \overline{A}C + A\overline{C} = A \oplus C$$

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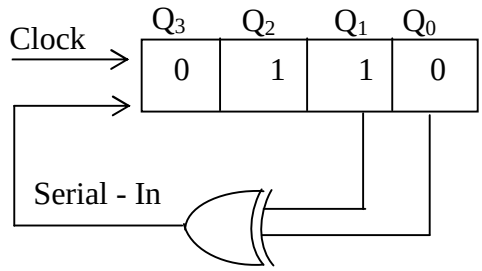
65. Ans: (c)

Sol:

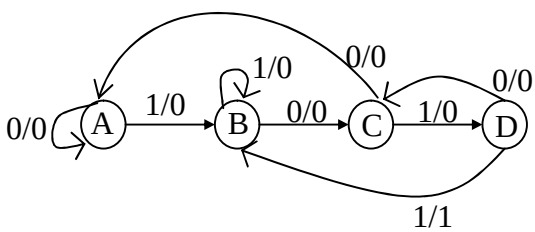


Serial In = $Q_1 \oplus Q_0$

CLK	Serial In	Q_3	Q_2	Q_1	Q_0
		0	1	1	0
1	1	1	0	1	1
2	0	0	1	0	1
3	1	1	0	1	0

66. Ans: (c)

Sol: The state diagram to detect the sequence 1011 is given below.



Total no. of states are = 4.

$\therefore$ 2 flip flops are required to detect the sequence 1011

67. Ans: (c)

Sol: TRAP has both edge & level sensitive.

68. Ans: (c)

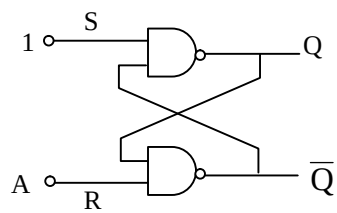
Sol: Vector Address for RST 4.5 = 4.5×8

$= 36$

$= 0024$ H

69. Ans: (d)

Sol: though oscillations are there when switch is closed, we need to get constant waveform without oscillations (bounce)



Fix 'S' at logic '1', connect A to 'R' input of S-R NAND latch

When A = 0 $\Rightarrow$ R = 0 $\Rightarrow$ $\overline{Q} = 1 \Rightarrow$ Q = 0

Now, even if A = 1 (due to bounce) i.e R = 1 $\Rightarrow$ Q remains in previous state i.e., (Q = 0)

70. Ans: (d)

Sol: In BJT as temperature increasing I_{co} increases So, I_c increases.

Where in FET, As temperature increases mobility decreases So I_D decreases and as temperature increases carrier concentration n_i increases so I_D increases.

So overall I_D will not get changed.

Thermal stability in FET is more than BJT

Parameter variation with temperature change is less.

71. Ans: (a)

Sol: Using A S C I I, we can represent data in both numbers and characters

72. Ans: (a)

73. Ans: (d)

74. Ans: (b)

Sol: The gain of the CE amplifier at low frequencies depend on the coupling, bypass and blocking capacitors and independent of interelectrode capacitances.

75. Ans: (a)